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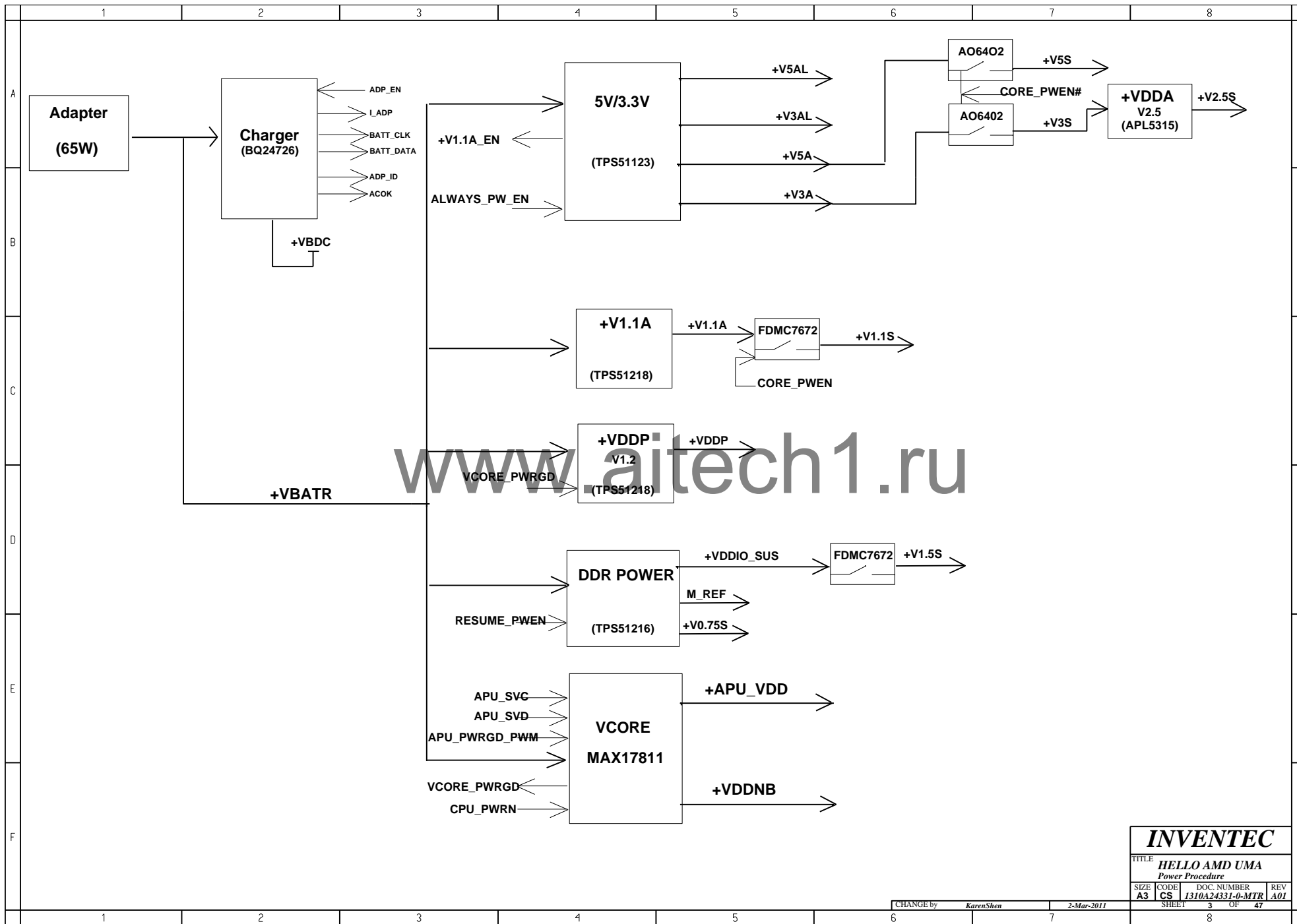
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**INVENTEC**

TITLE <b>HELLO AMD UMA</b>			
Index			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A24331-0-MTR</b>	REV <b>A01</b>
SHEET <b>2</b>		OF <b>47</b>	

CHANGE by *KarenShen* 2-Mar-2011



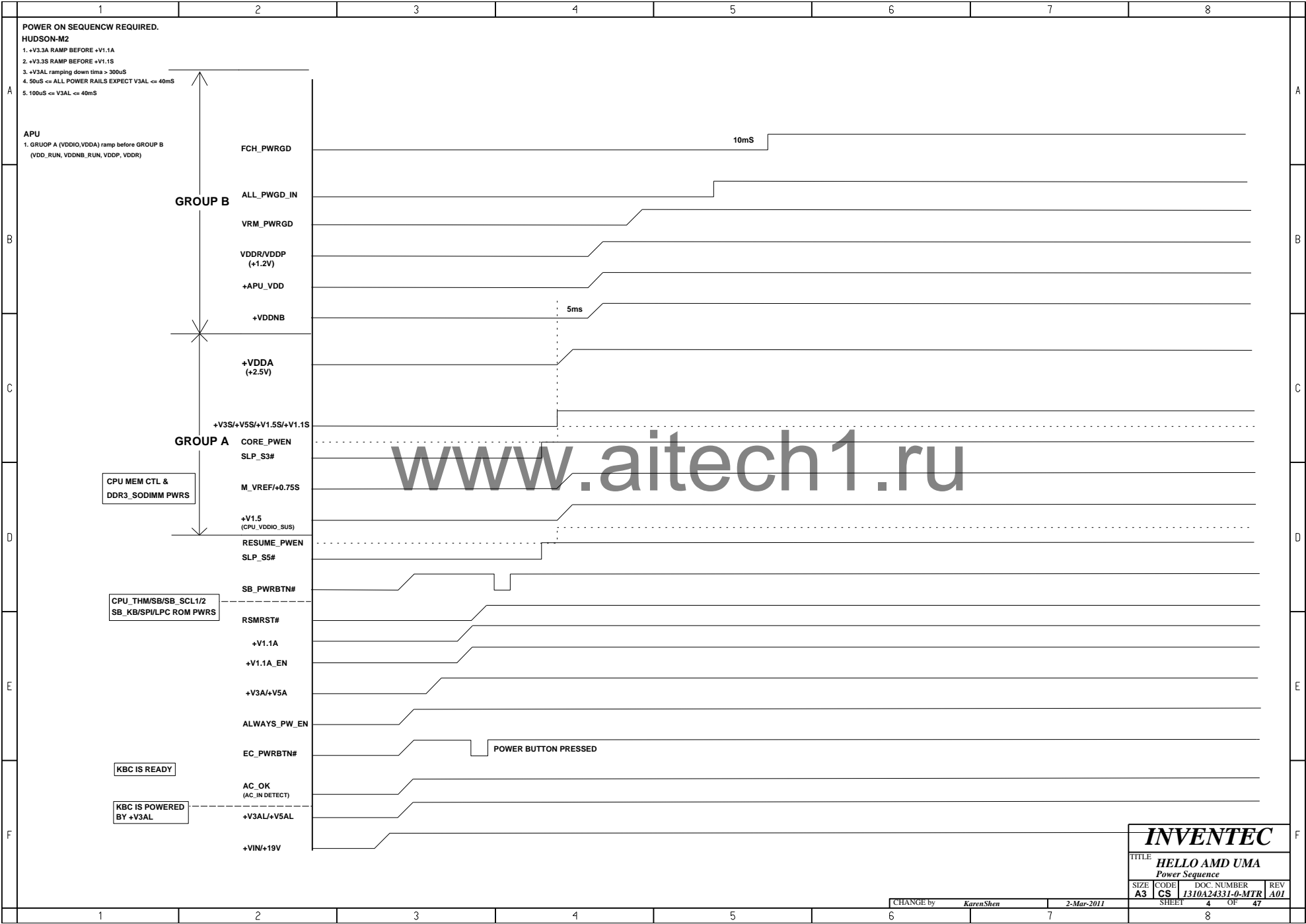
**INVENTEC**

TITLE: **HELLO AMD UMA**  
Power Procedure

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24331-0-MTR	A01

CHANGE by: *KarenShen* 2-Mar-2011

SHEET 3 OF 47



INVENTEC

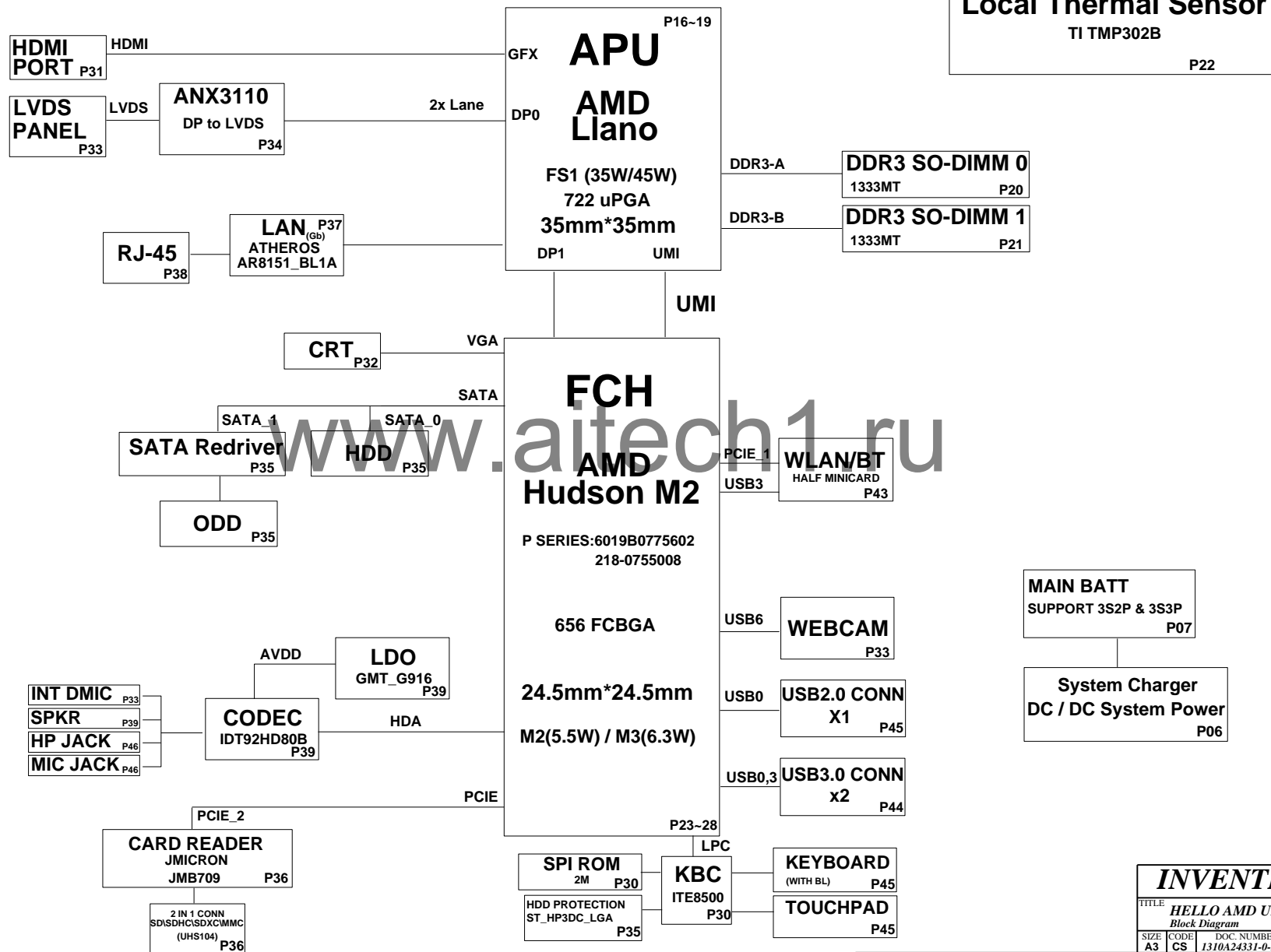
TITLE  
HELLO AMD UMA  
Power Sequence

SIZE A3	CODE CS	DOC. NUMBER 1310A24331-0-MTR	REV A01
SHEET 4		OF 47	

CHANGE by KarenShen 2-Mar-2011

Inventec Confidential

Sabine - UMA (only)



INVENTEC

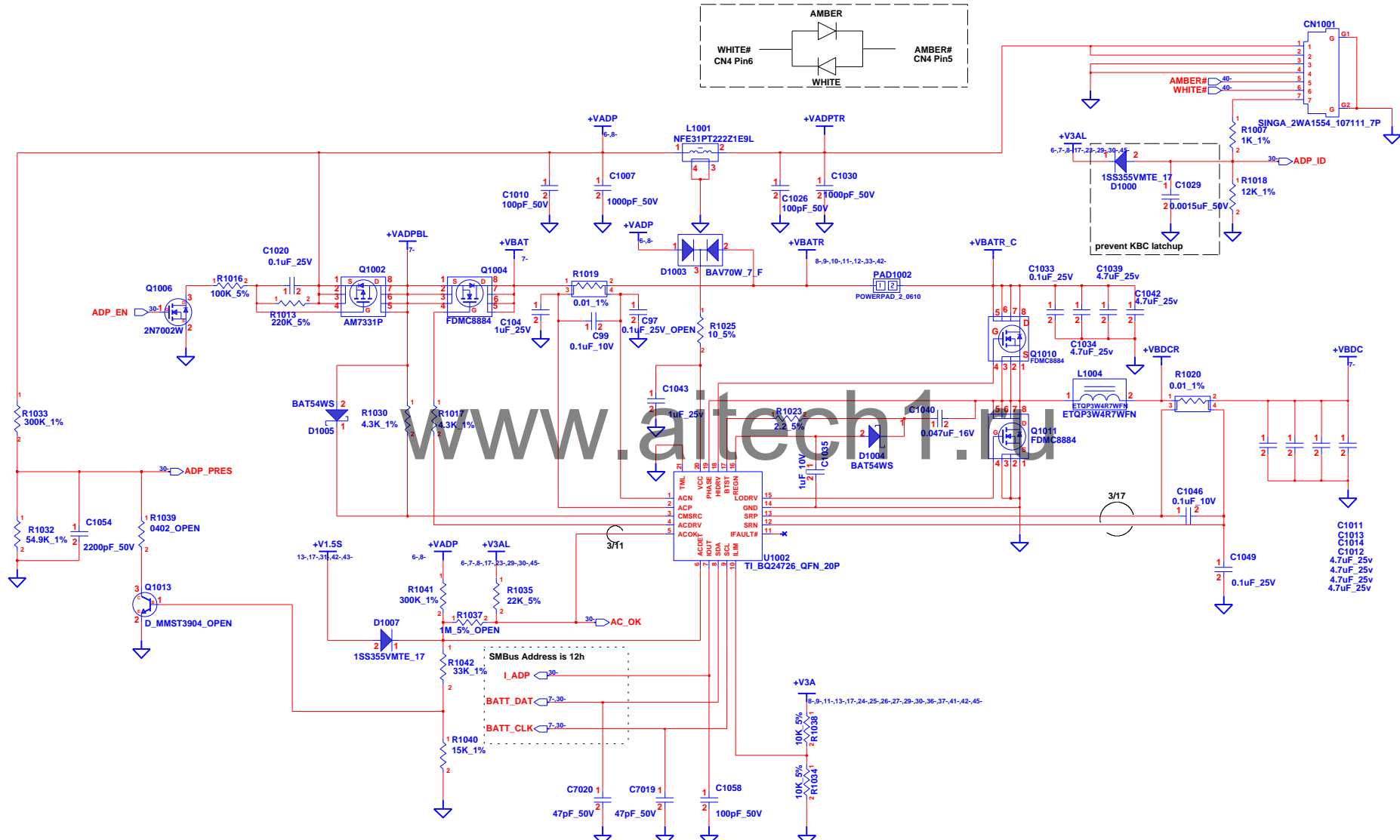
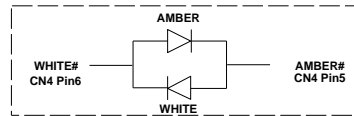
TITLE: HELLO AMD UMA  
Block Diagram

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24331-0-MTR	A01

CHANGE by KarenShen 2-Mar-2011

SHEET 5 OF 47

AC IN

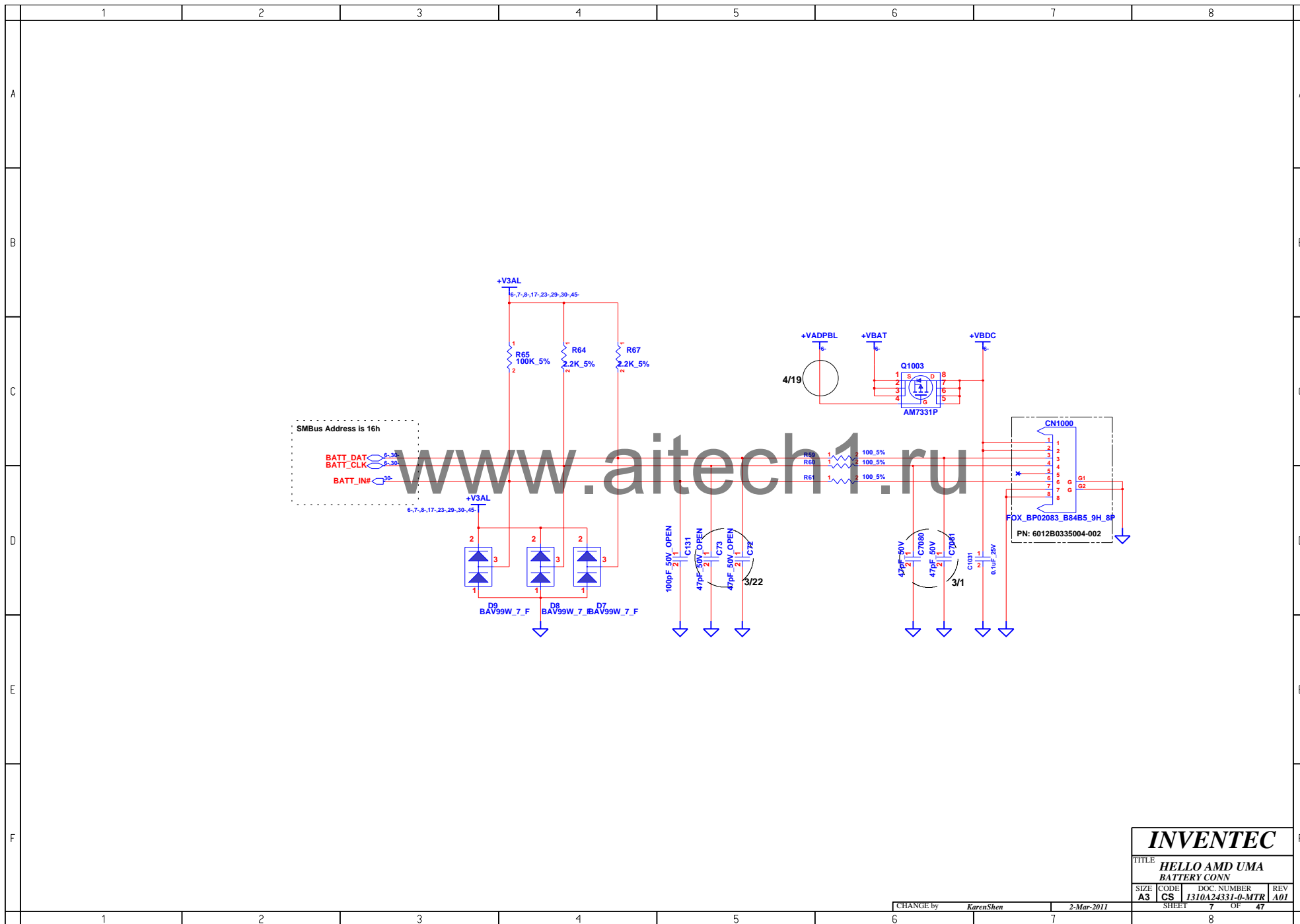


INVENTEC

TITLE HELLO AMD UMA DC & BATTERY CHARGER			
SIZE A3	CODE CS	DOC NUMBER 1310A24331-0-MTR	REV A01

CHANGE by KarenShen 2-Mar-2011

SHEET 6 OF 47



**INVENTEC**

TITLE  
**HELLO AMD UMA  
BATTERY CONN**

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A24331-0-MTR</b>	REV <b>A01</b>
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CHANGE by *KarenShen* 2-Mar-2011

SHEET 7 OF 47

3



0A24331-0-M1R

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8 OF 47



## A



2

D

F

F

CHANGE by	<i>Karen Shen</i>	2-Mar-2011
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[illegible]

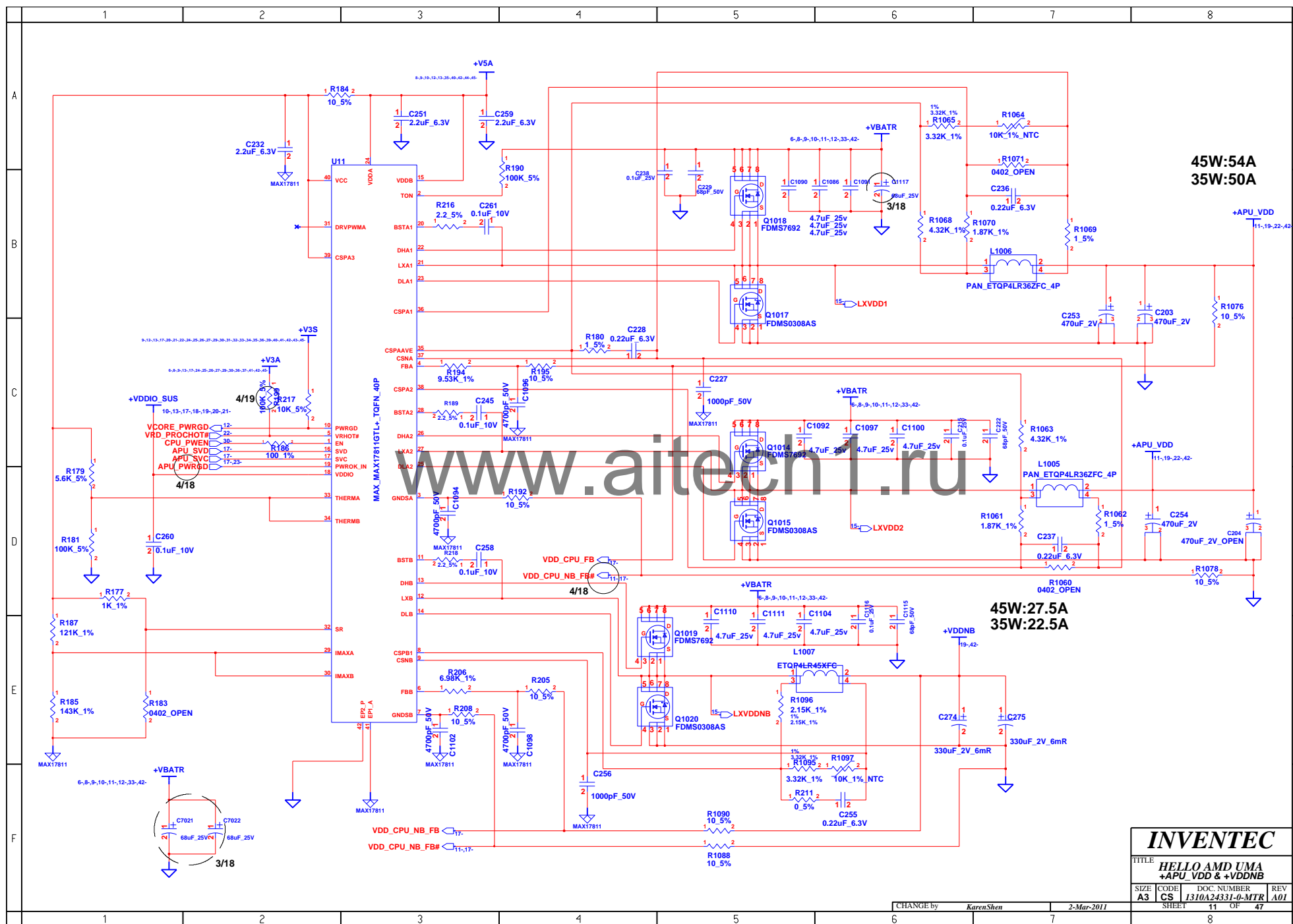
**VDDIO\_SUS & +V0.75S**

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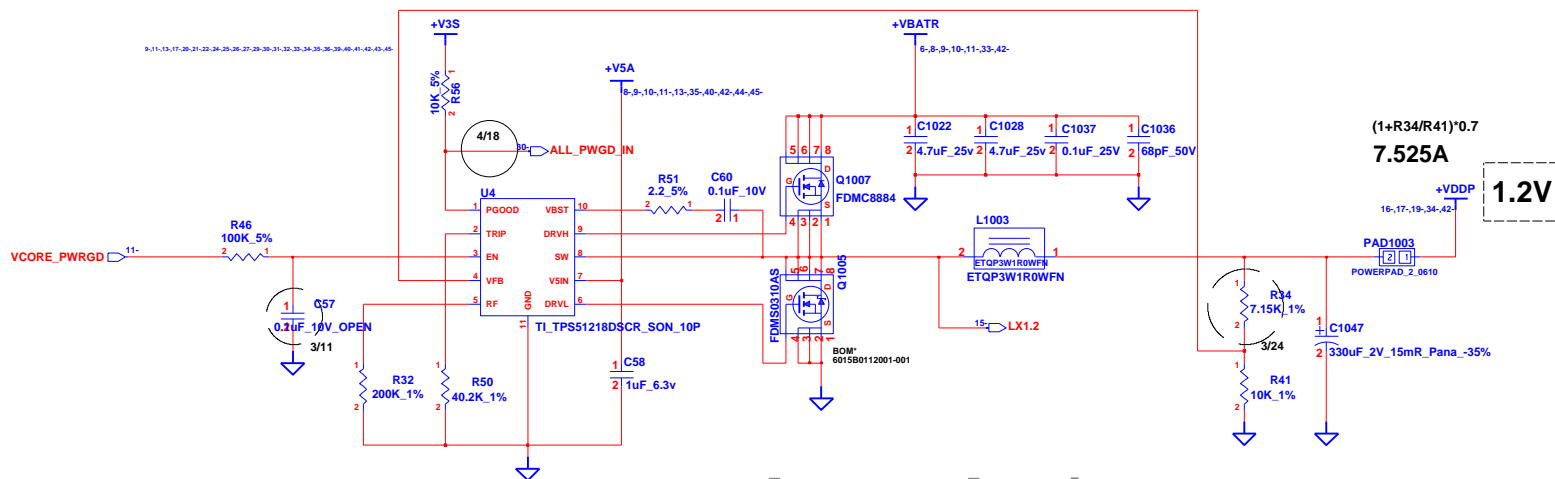
**VDDIO\_SUS & +V0.75S**

**VDDIO\_SUS & +V0.75S**

[illegible][illegible]



# +VDDP



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**INVENTEC**

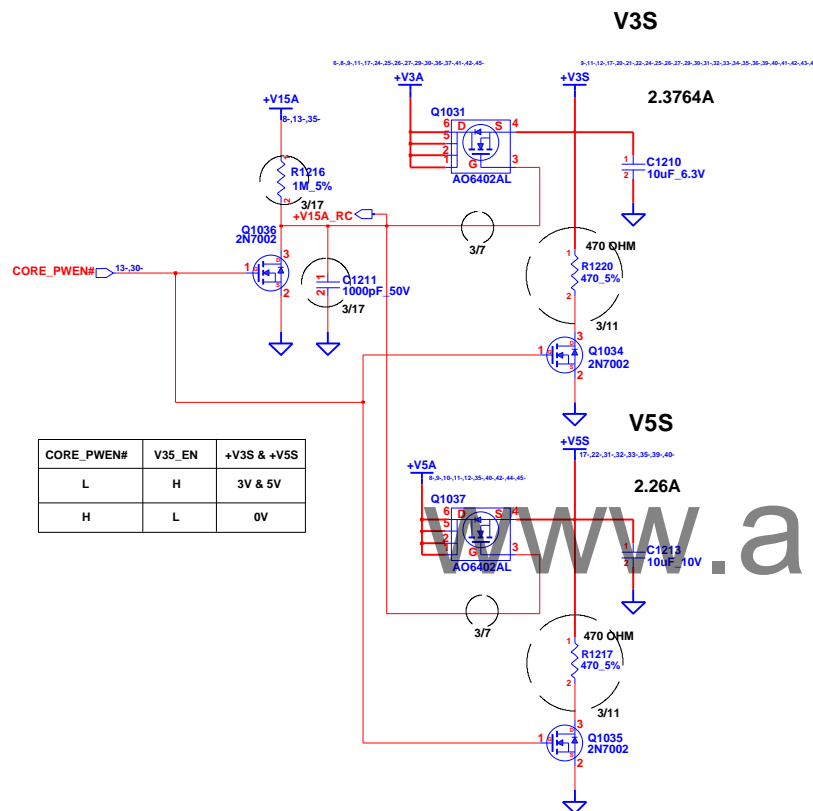
TITLE: **HELLO AMD UMA**  
+VDDP & +V1.8S\_GPU

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24331-0-MTR	A01

CHANGE by: KarenShen 2-Mar-2011

SHEET 12 OF 47

# +V5S & +V3S & +V1.5S & +V1.1S



CORE_PWEN#	V3S_EN	+V3S & +V5S
L	H	3V & 5V
H	L	0V

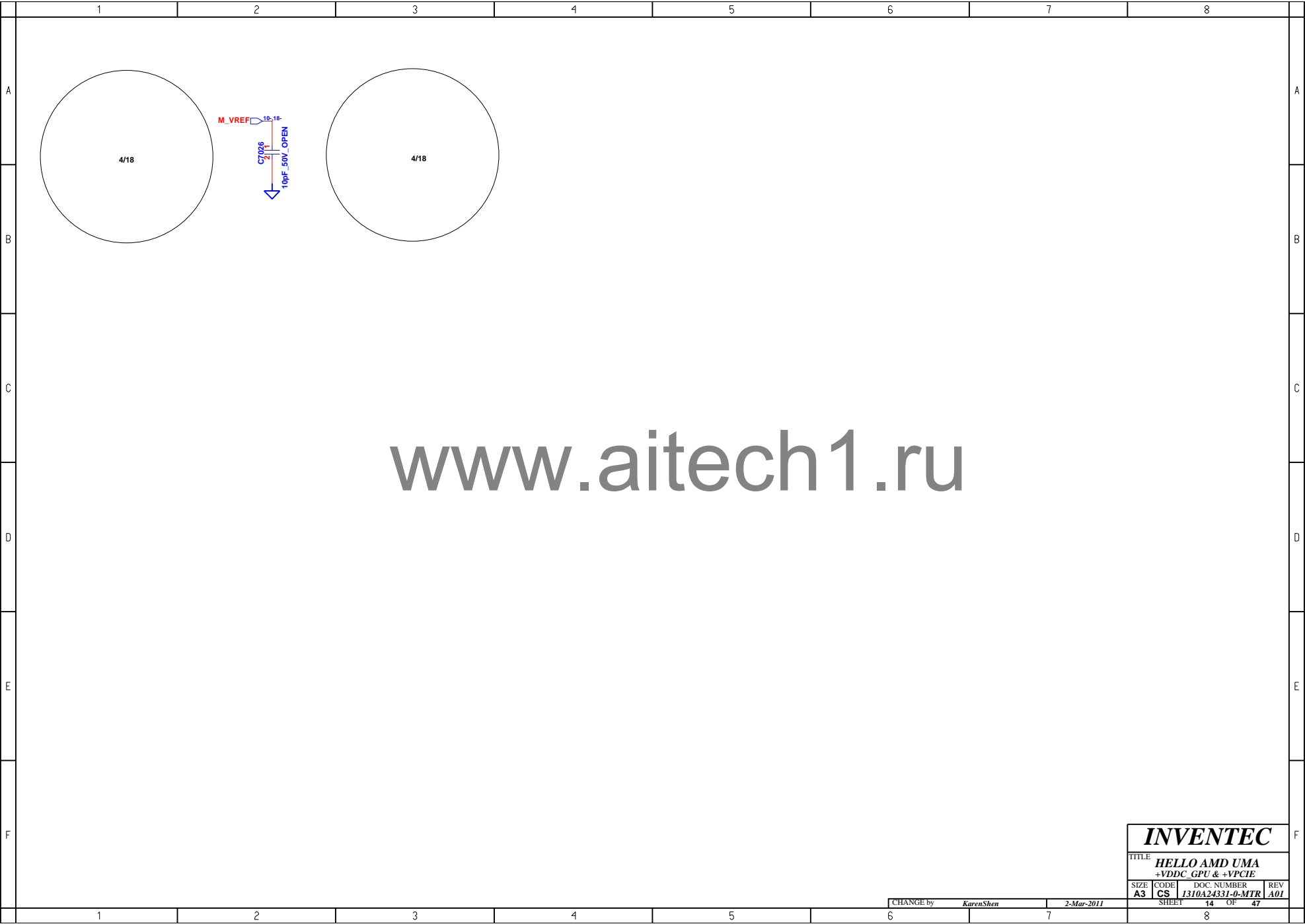
www.aitech1.ru

**INVENTEC**

TITLE			
HELLO AMD UMA			
+V5S & +V3S & +V1.5S & +V1.1S			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24331-0-MTR	A01

CHANGE by KarenShen 2-Mar-2011

SHEET 13 OF 47



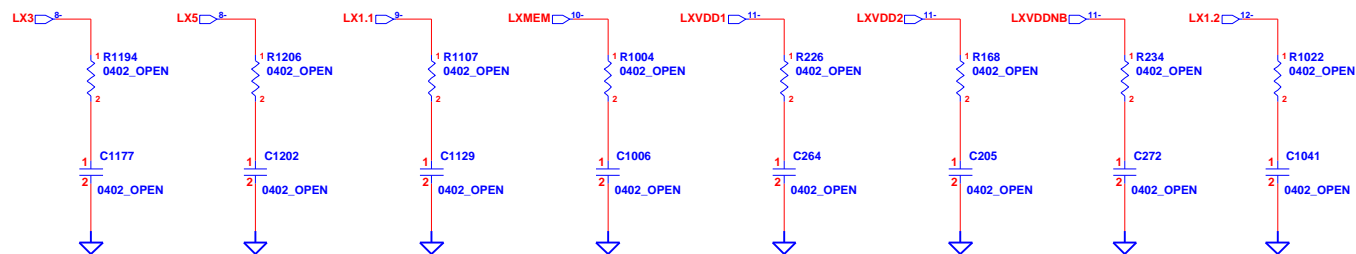
**INVENTEC**

TITLE **HELLO AMD UMA**  
**+VDDC\_GPU & +VPCIE**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24331-0-MTR	A01

CHANGE by *KarenShen* 2-Mar-2011

SHEET 14 OF 47

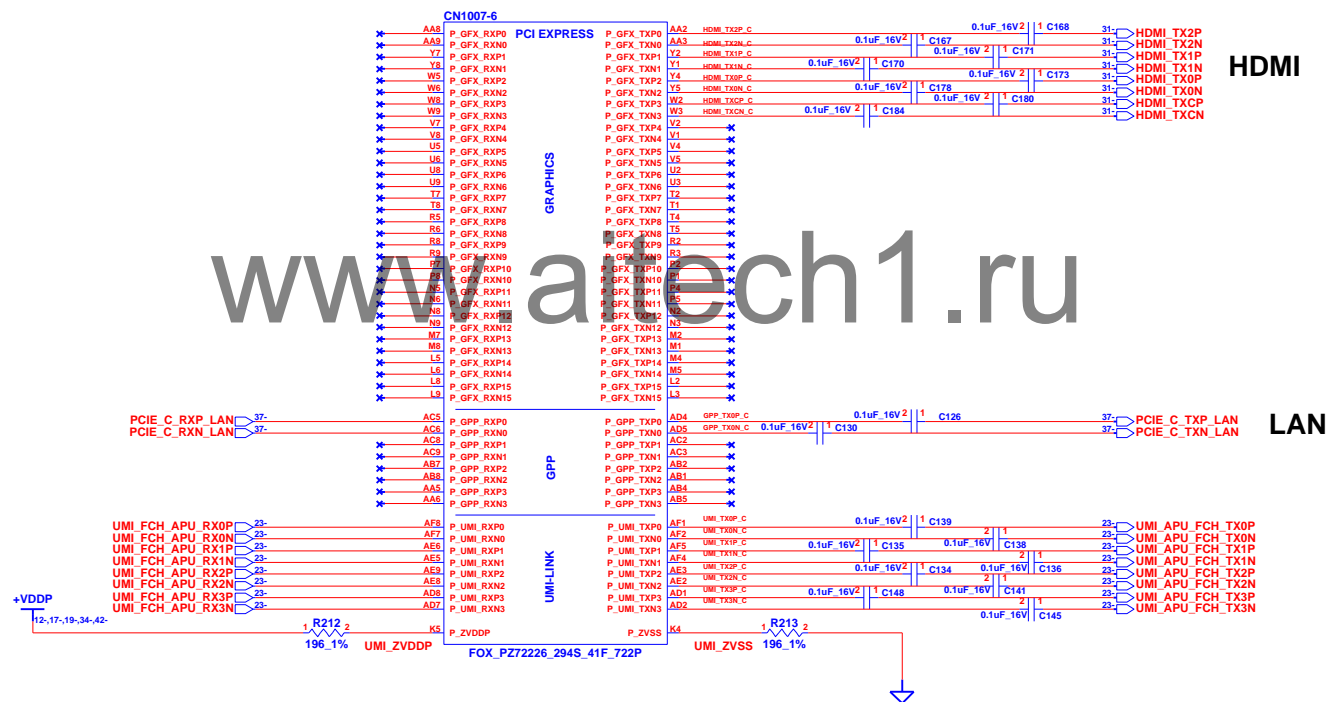


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INVENTEC			
TITLE HELLO AMD UMA			
SIZE A3	CODE CS	DOC. NUMBER 1310A24331-0-MTR	REV A01
CHANGE by KarenShen		2-Mar-2011	
SHEET 15		OF 47	

# CPU

(6026B0194402)  
\*BOM



**INVENTEC**

TITLE  
**HELLO AMD UMA**  
CPU-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24331-0-MTR	A01

CHANGE by *KarenShen* 2-Mar-2011

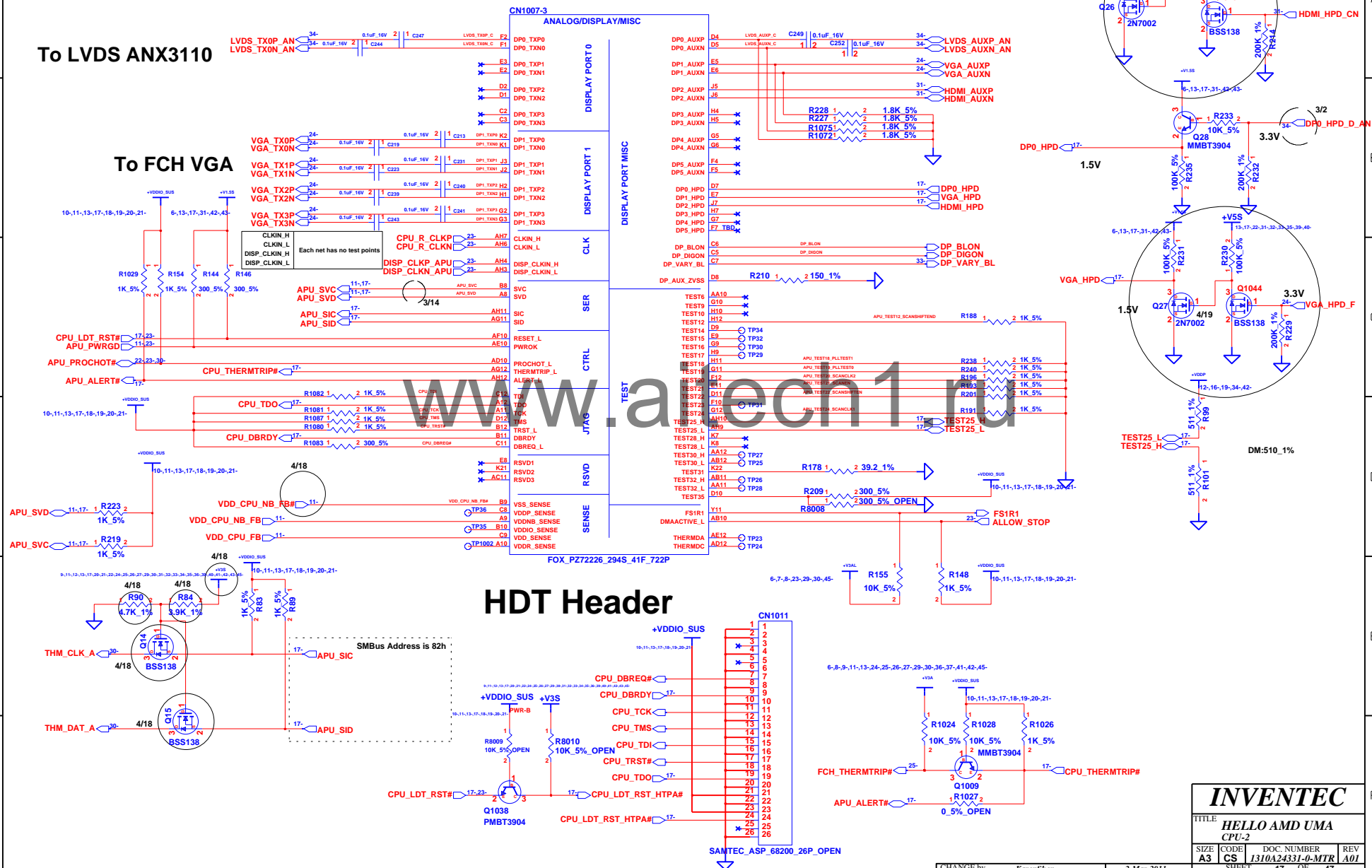
SHEET 16 OF 47



# CPU

## To LVDS ANX3110

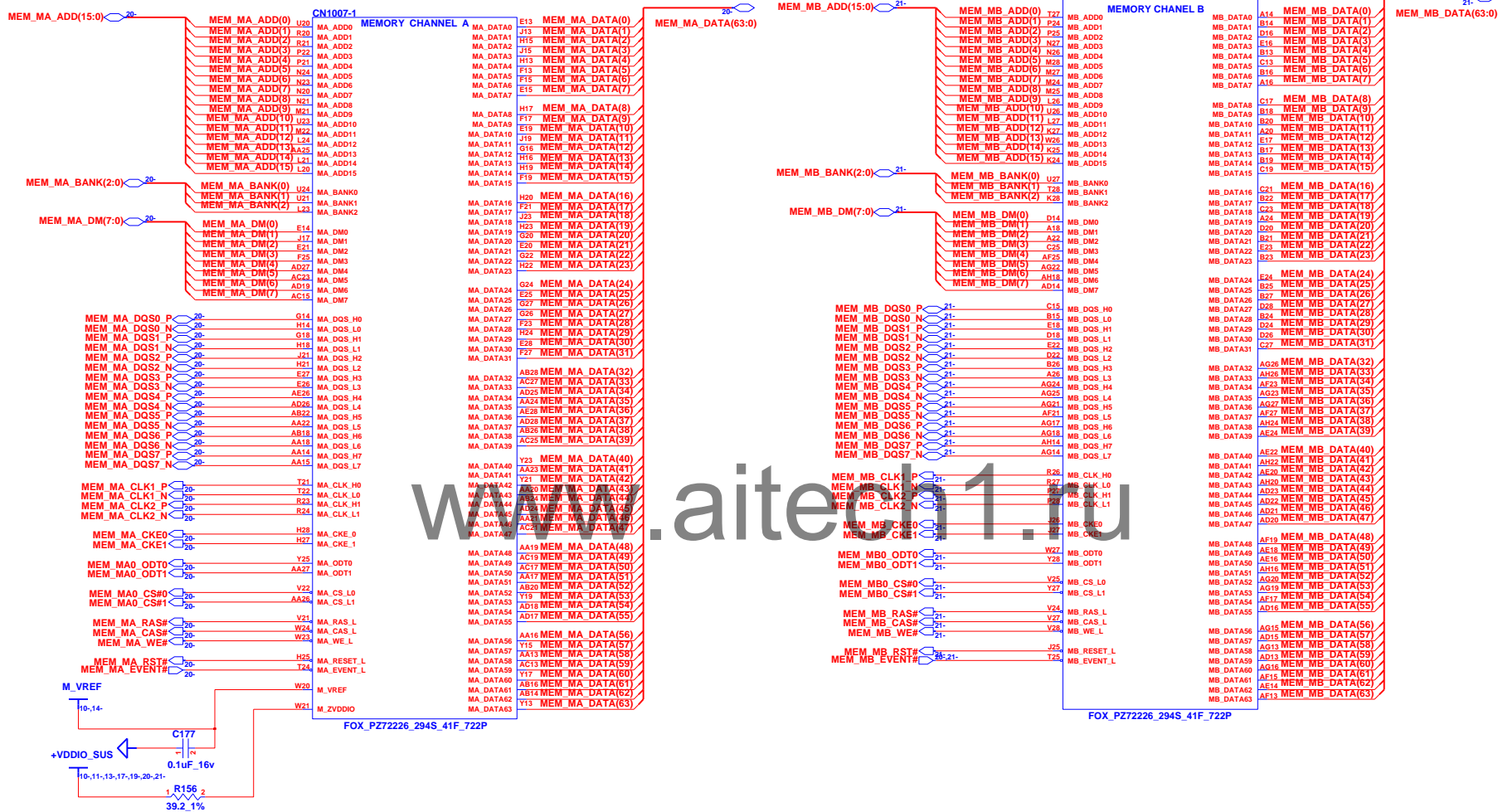
**To FCH VGA**



## HDT Header

<b>INVENTEC</b>			
TITLE <b>HELLO AMD UMA</b>			
<b>CPU-2</b>			
SIZE	CODE	DOC. NUMBER	REV
<b>A3</b>	<b>CS</b>	<b>1310A24331-0-MTR</b>	<b>A01</b>

# CPU



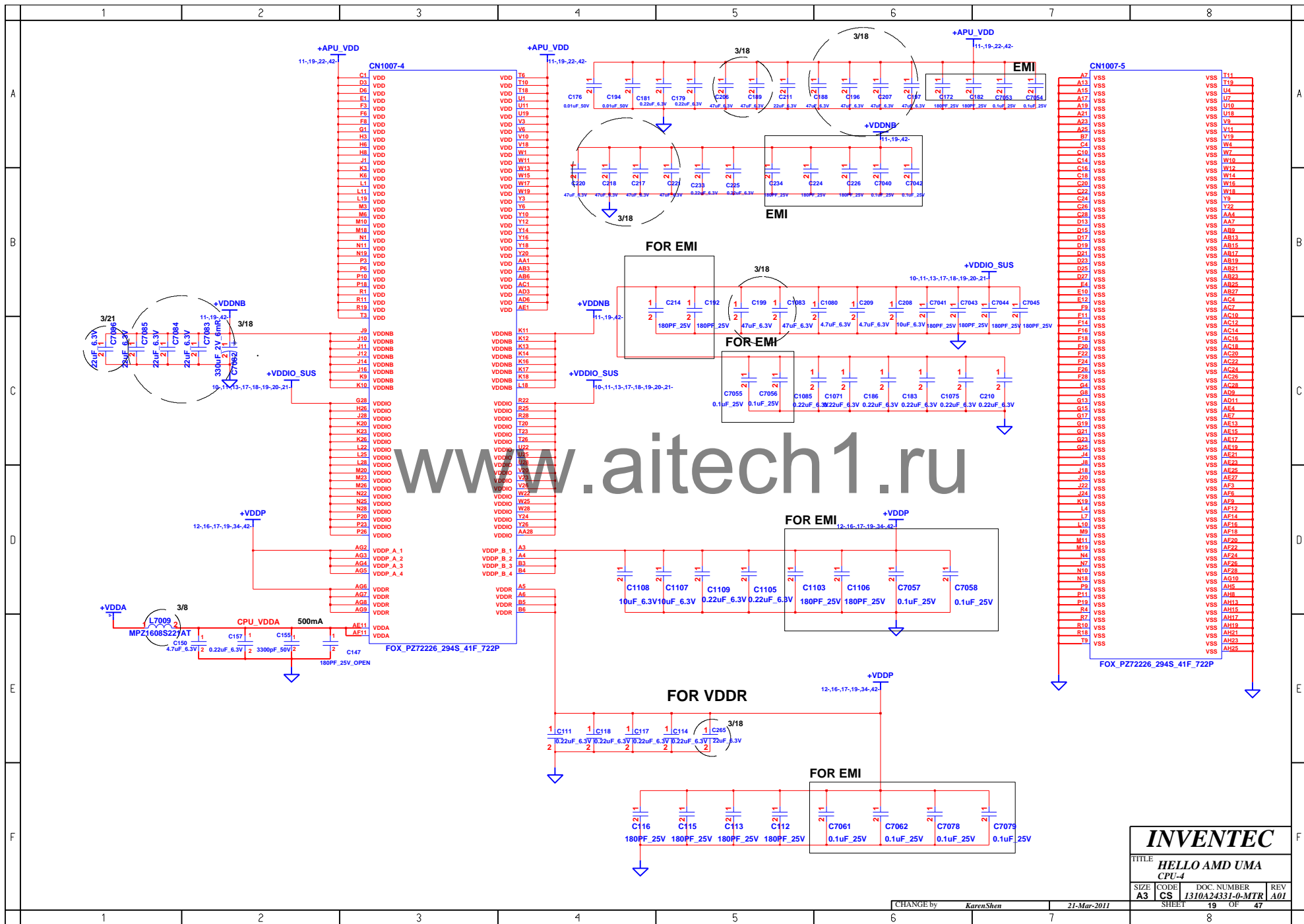
**INVENTEC**

TITLE: HELLO AMD UMA  
CPU-3

SIZE: A3 CODE: CS DOC. NUMBER: 1310A24331-0-MTR REV: A01

SHEET: 18 OF 47

CHANGE by: KarenShen 2-Mar-2011



**INVENTEC**

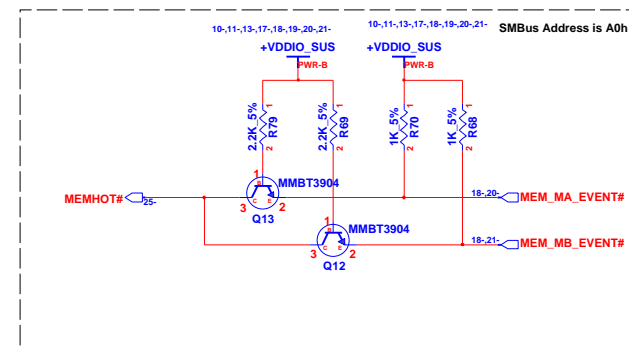
TITLE: **HELLO AMD UMA**  
CPU-4

SIZE: **A3** CODE: **CS** DOC. NUMBER: **1310A24331-0-MTR** REV: **A01**

CHANGE by: **KarenShen** 21-Mar-2011

SHEET: **19** OF **47**

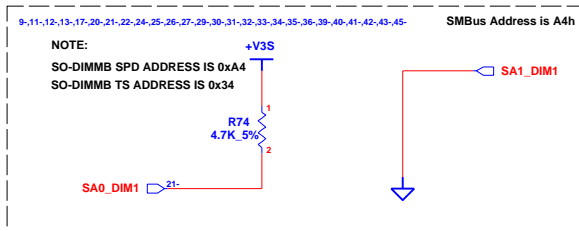
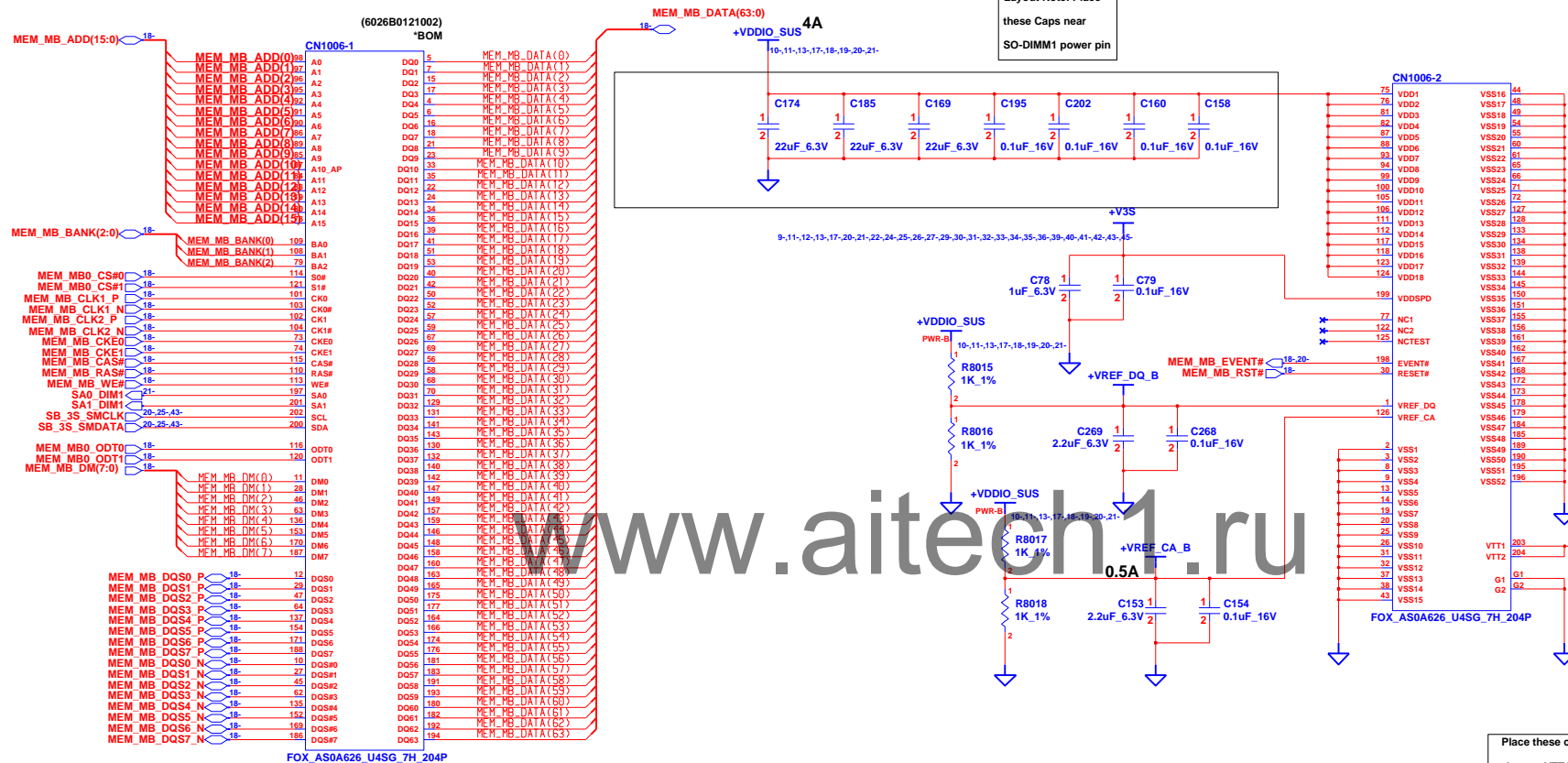
MEM_MA_ADD(15:0)		CN1005-1		"BOM"	
MEM_MA_ADD(15:0)	1B	MEM_MA_ADD(0)	38	D0	5
		MEM_MA_ADD(1)	92	D1	7
		MEM_MA_ADD(2)	92	D2	15
		MEM_MA_ADD(3)	95	D3	17
		MEM_MA_ADD(4)	92	D4	6
		MEM_MA_ADD(5)	92	D5	16
		MEM_MA_ADD(6)	91	D6	4
		MEM_MA_ADD(7)	86	D7	21
		MEM_MA_ADD(8)	86	D8	38
		MEM_MA_ADD(9)	85	D9	23
		MEM_MA_ADD(10)	107	D10	33
		MEM_MA_ADD(11)	107	D11	35
		MEM_MA_ADD(12)	84	D12	22
		MEM_MA_ADD(13)	119	D13	24
		MEM_MA_ADD(14)	80	D14	36
		MEM_MA_ADD(15)	78	D15	39
			A10	D16	39
			A11	D17	41
			A11	D18	53
			A11	D19	40
			A11	D20	56
			A11	D21	57
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			A11	D28	57
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			A11	D82	57
			A11	D83	57
			A11	D84	57
		</			



CHANGE by	<i>Karen Shen</i>	<i>2-Mar-2011</i>
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# SO-DIMM1-ST\_400

Layout Note: Place  
these Caps near  
SO-DIMM1 power pin



**INVENTEC**

TITLE  
HELLO AMD UMA  
SO-DIMM1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24331-0-MTR	A01

CHANGE by KarenShen 2-Mar-2011

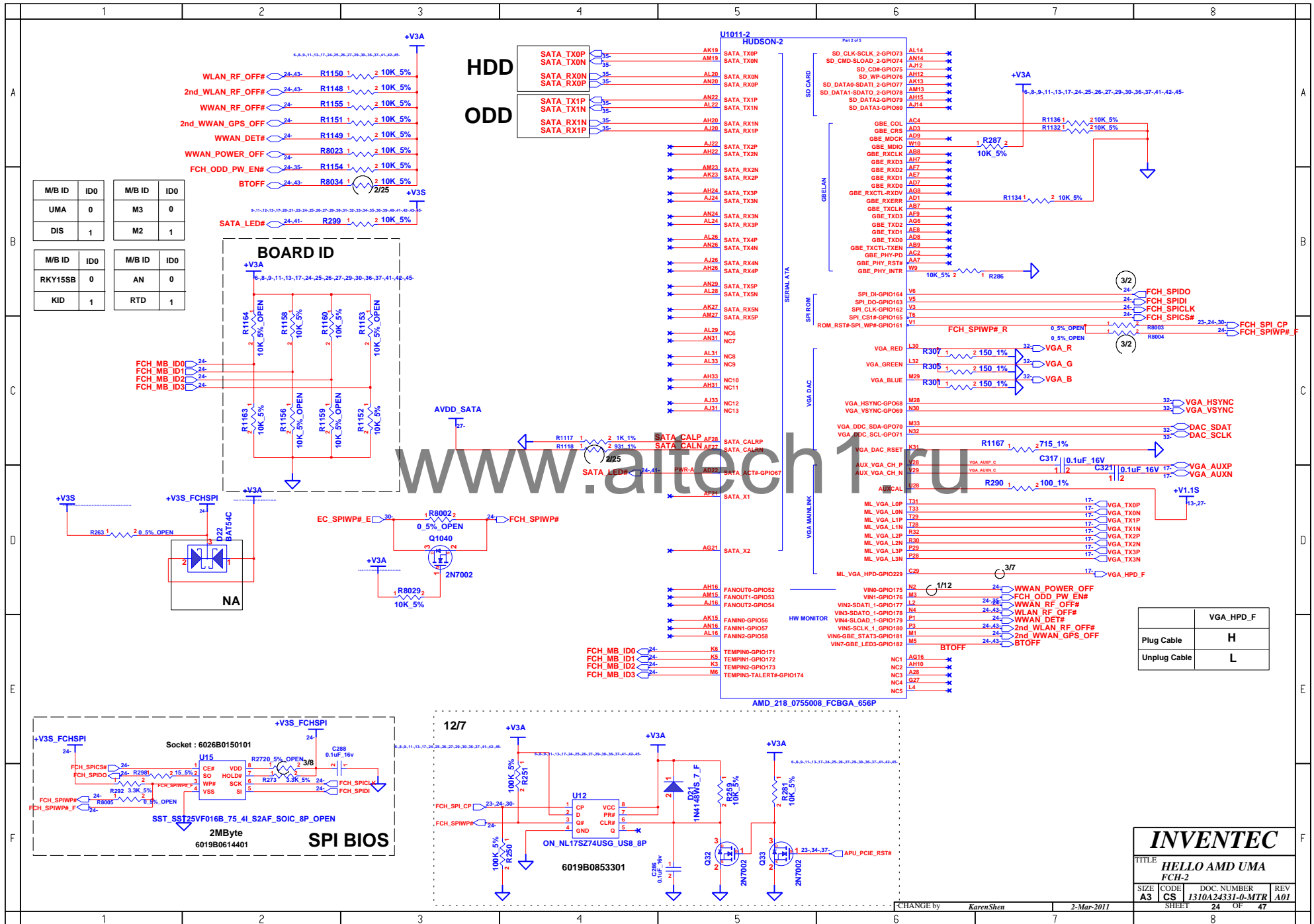
SHEET 21 OF 47



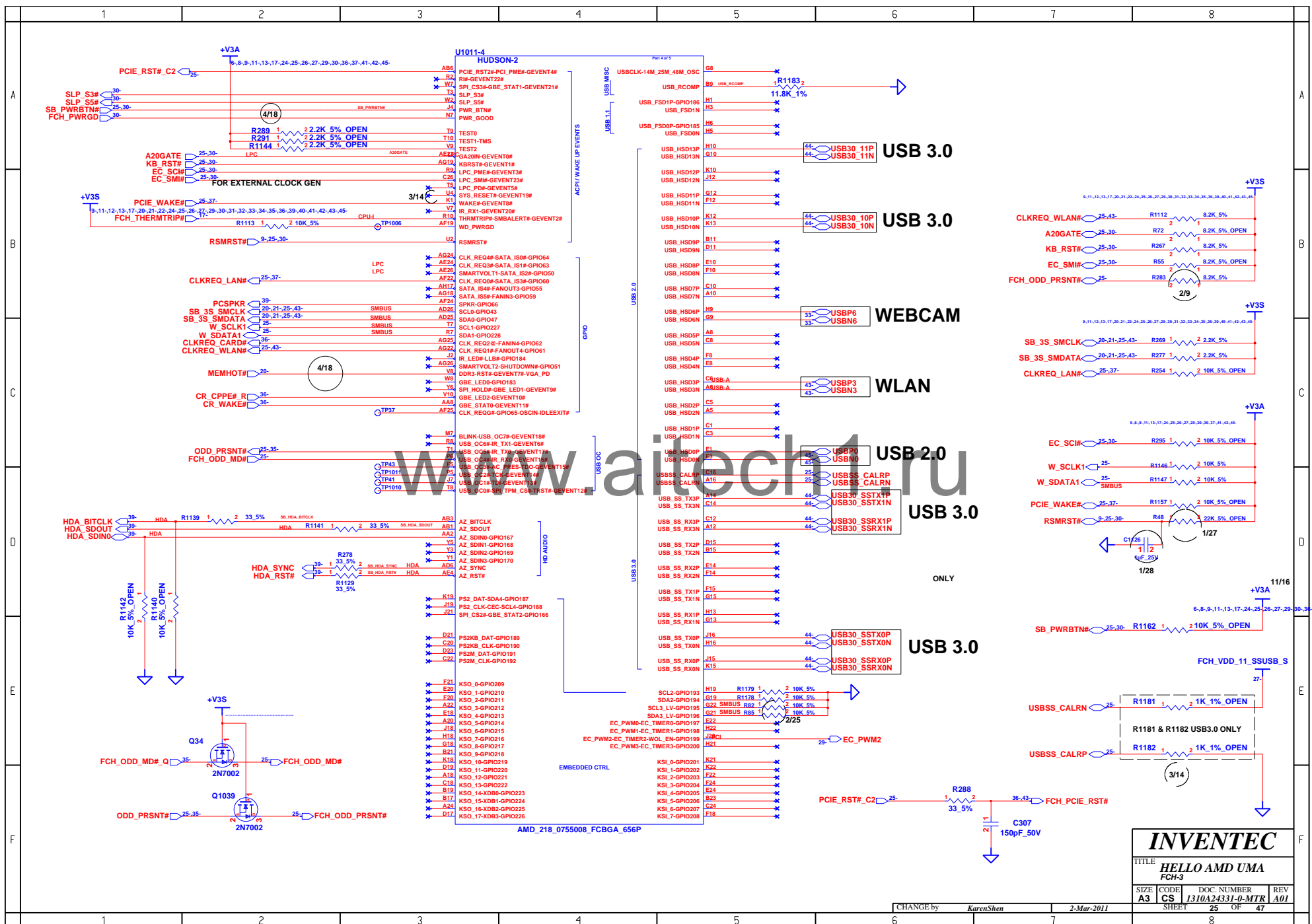
CHANGE by	<i>KarenShen</i>	<i>2-Mar-2011</i>
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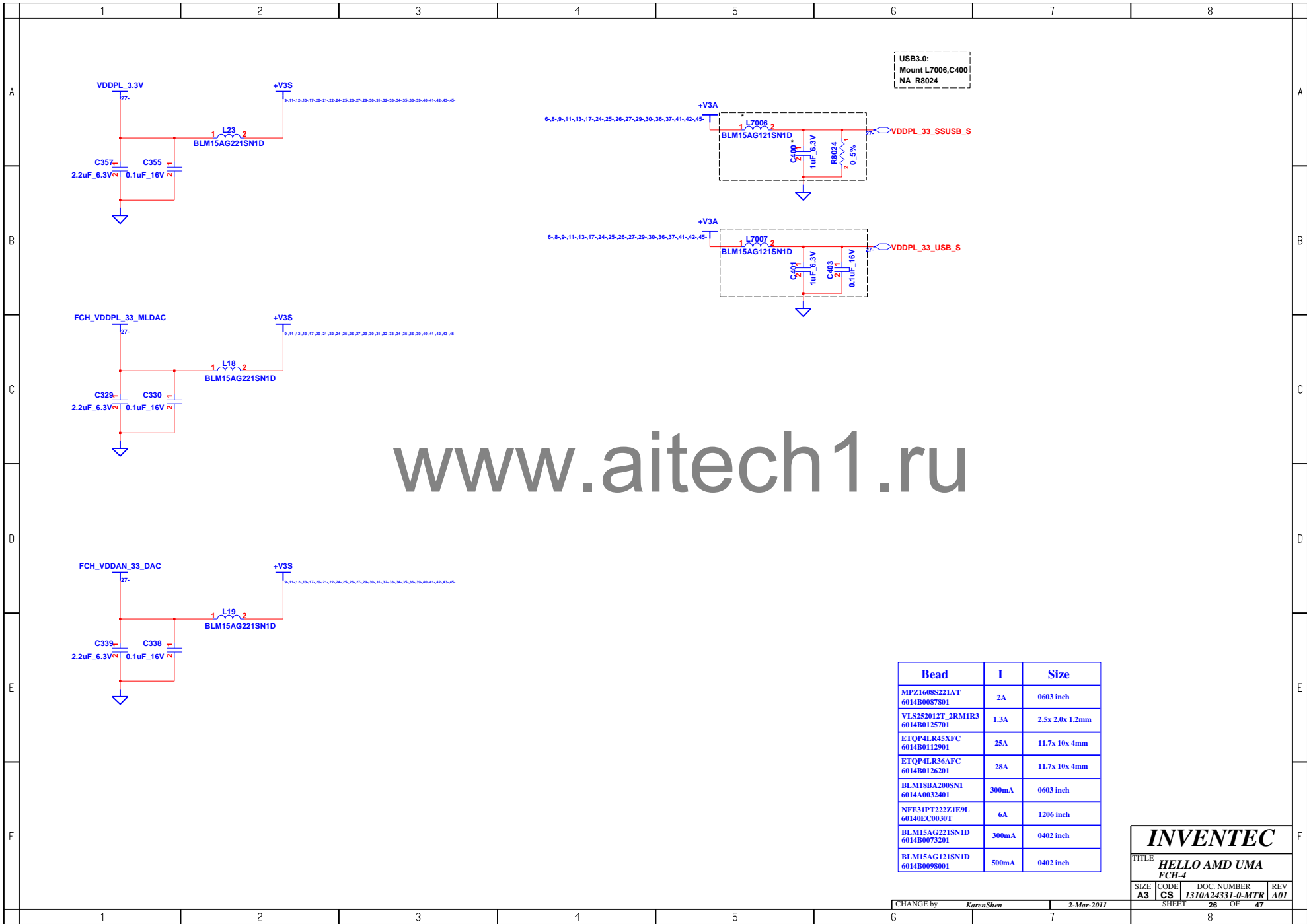


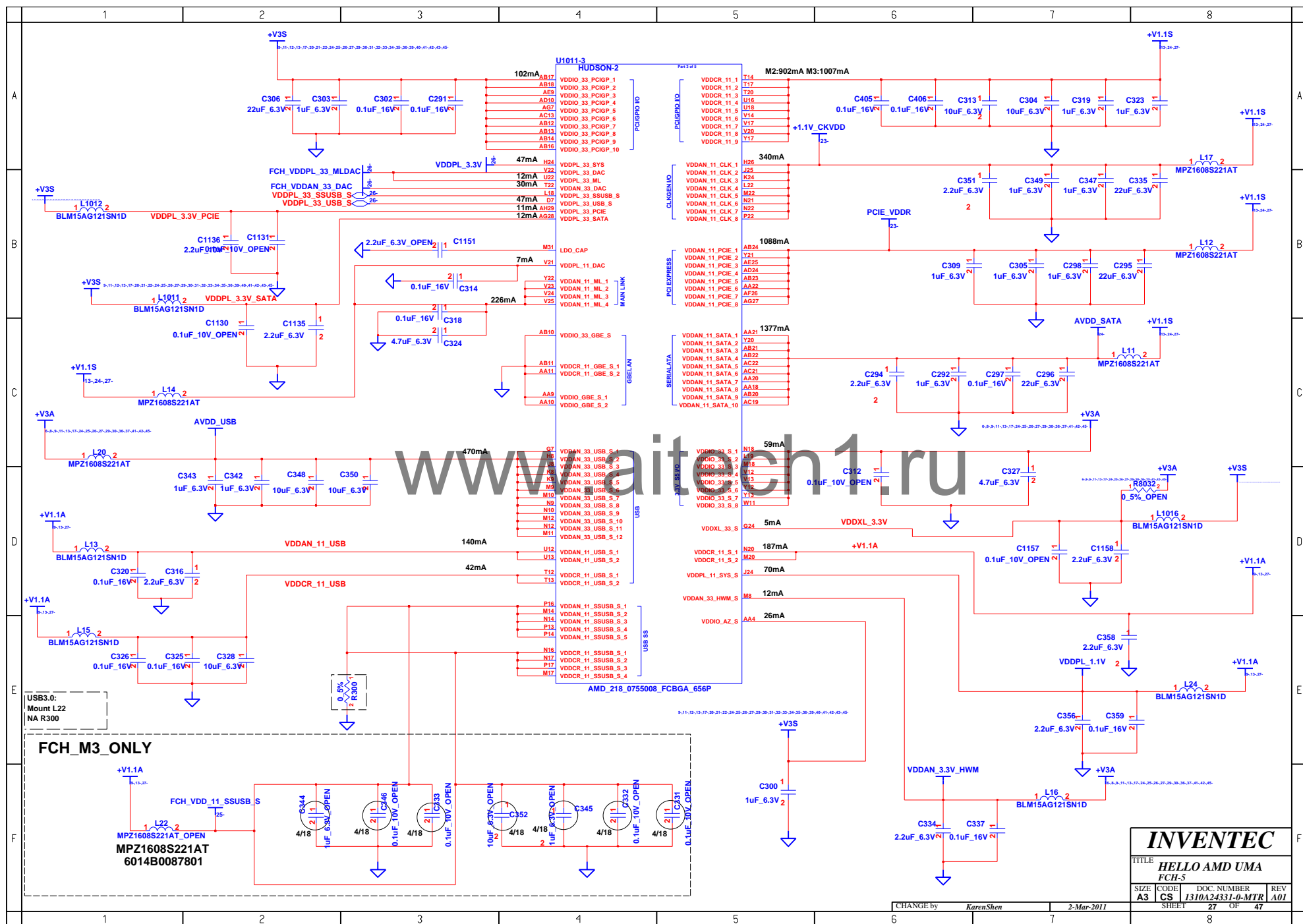


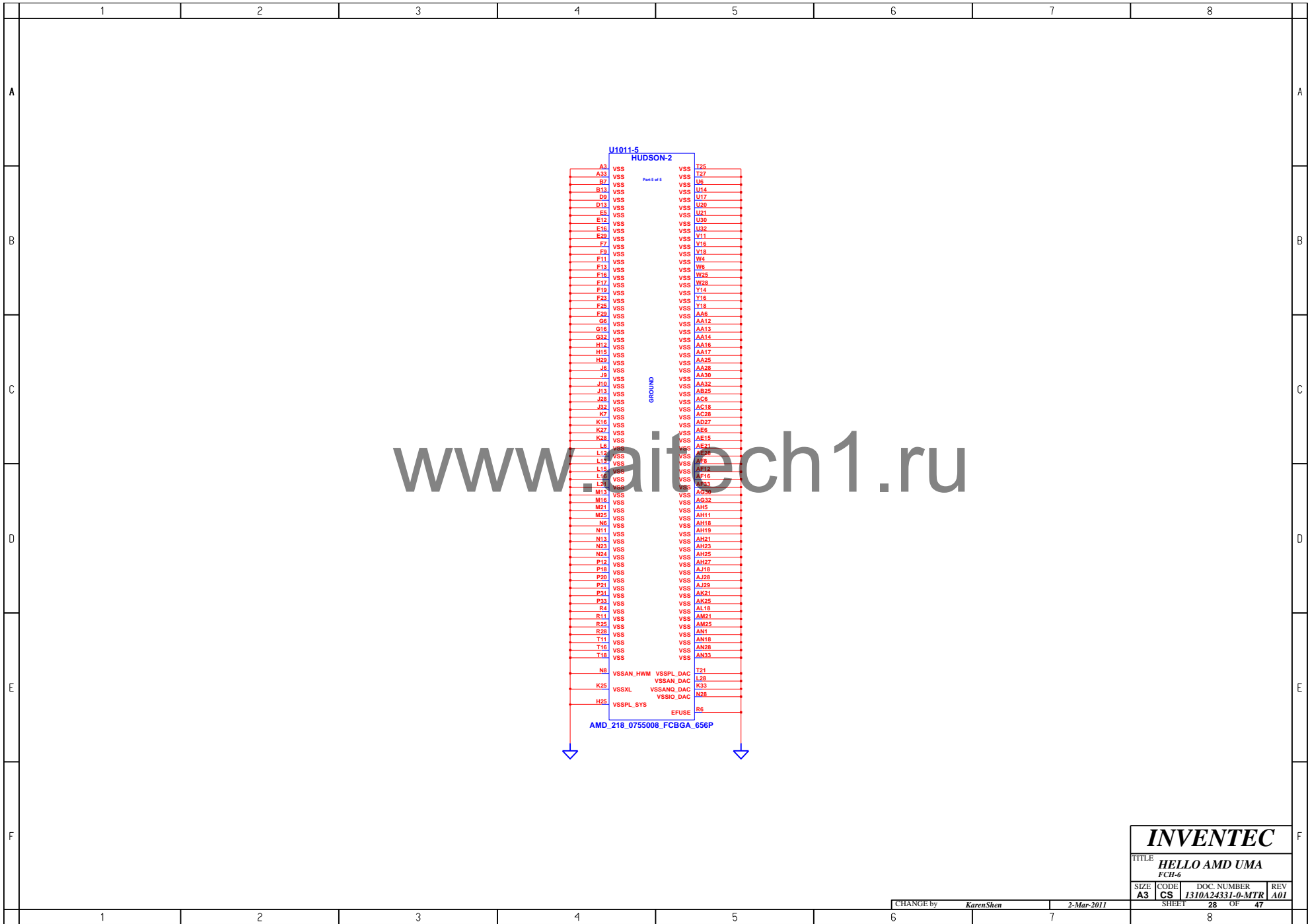


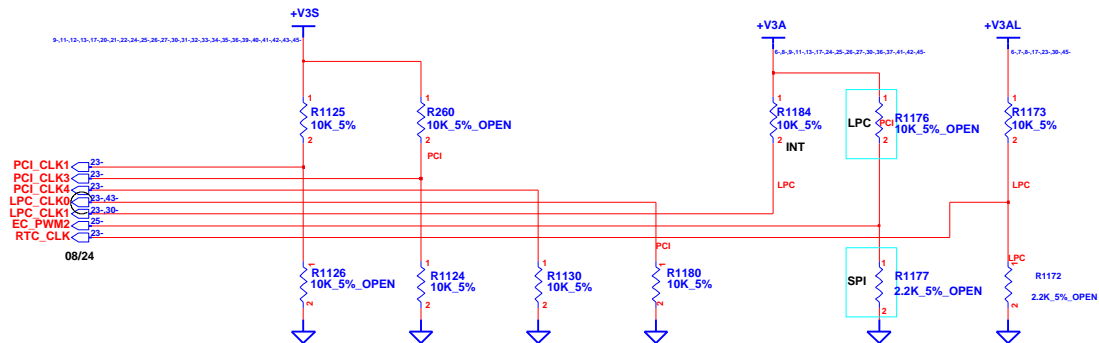








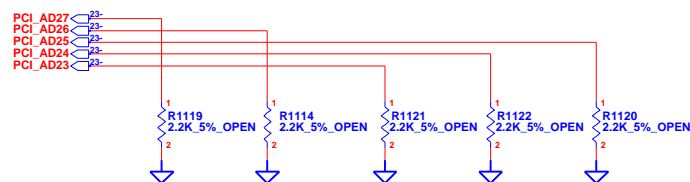




### Required Straps:

RTCCLK		PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2
S5 PLUS MODE DISABLE (DEFAULT)	<b>PULL HIGH</b>	ALLOW PCIE Gen2 DEFAULT	USE DEBUG STRAP	non Fusion CLOCK MODE APU_CLK AND DISP_CLK NO CLOCK OUTPUT	EC ENABLED	INTEGRATED CLKGEN ENABLED DEFAULT	LPC ROM
S5 PLUS MODE ENABLE	<b>PULL LOW</b>	FORCE PCIE Gen1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK MODE DEFAULT APU_CLK AND DISP_CLK CLOCK OUTPUT FROM INT CLOCK GEN	EC DISABLED DEFAULT	INTEGRATED CLKGEN DISABLED	SPI ROM DEFAULT

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### Debug Straps

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

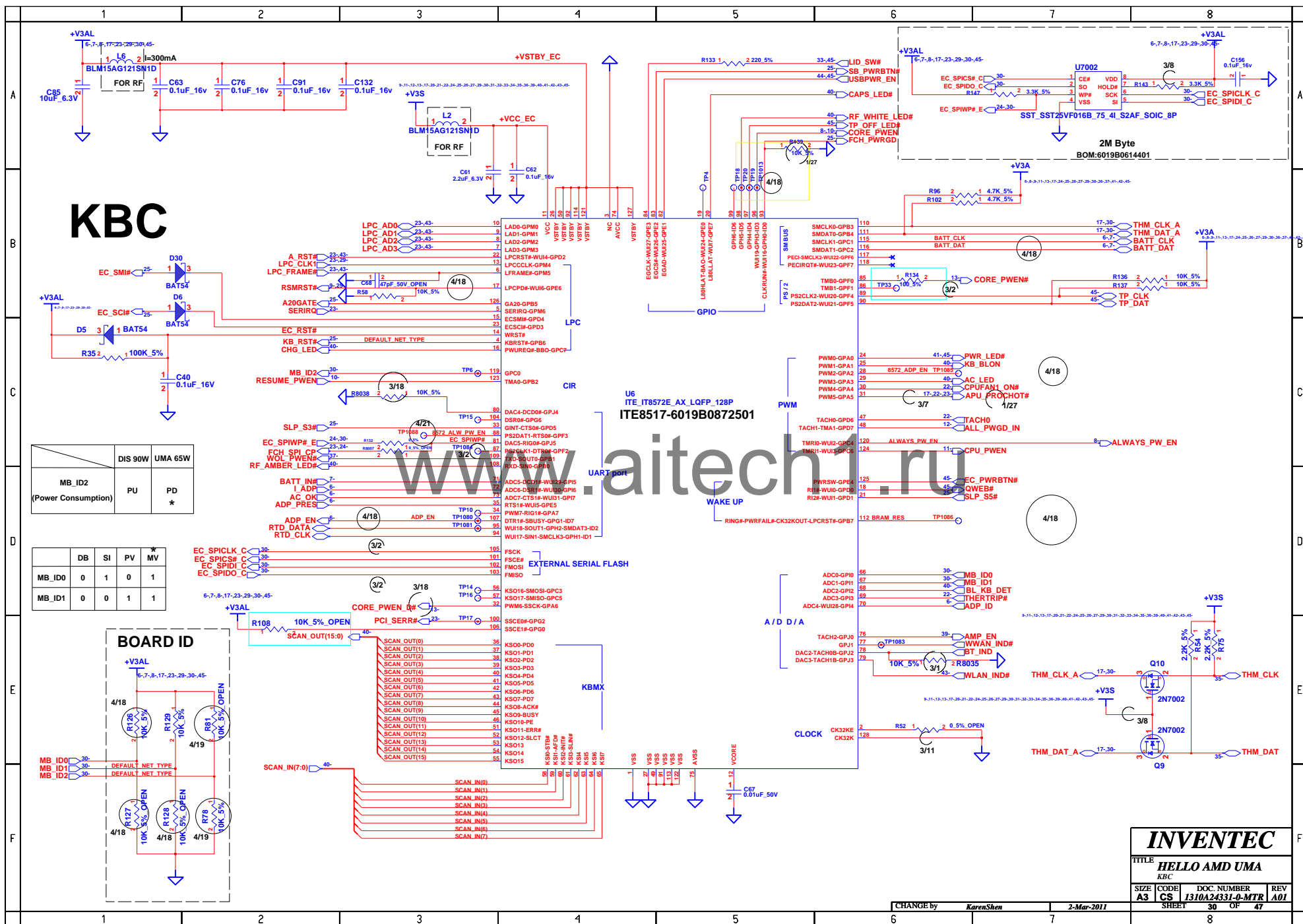
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL (default)	DISABLE ILA AUTORUN (default)	USE FC PLL (default)	USE DEFAULT PCIE STRAPS (default)	DISABLE PCI MEM BOOT (default)
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PCI PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

**INVENTEC**

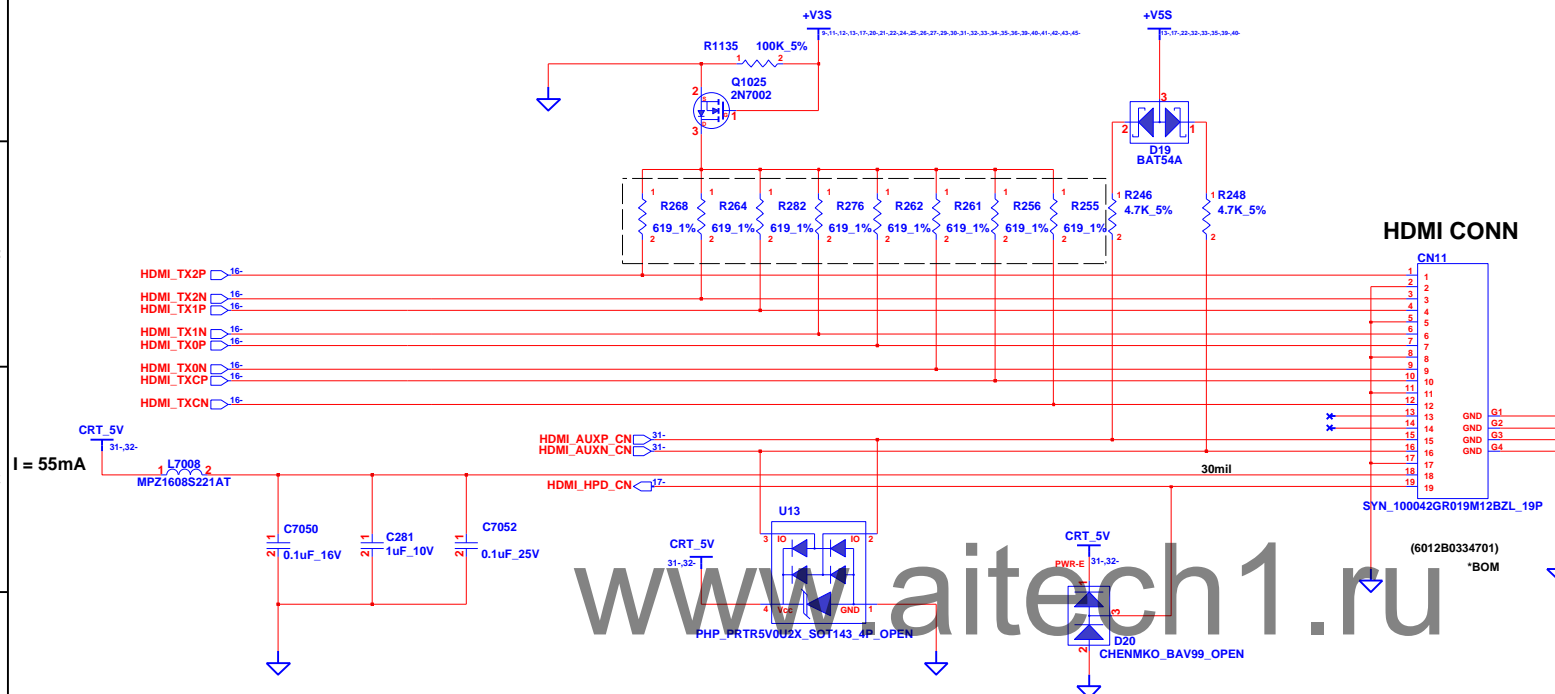
TITLE  
**HELLO AMD UMA  
STRAP**

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A24331-0-MTR</b>	REV <b>A01</b>
SHEET <b>29</b>		OF <b>47</b>	

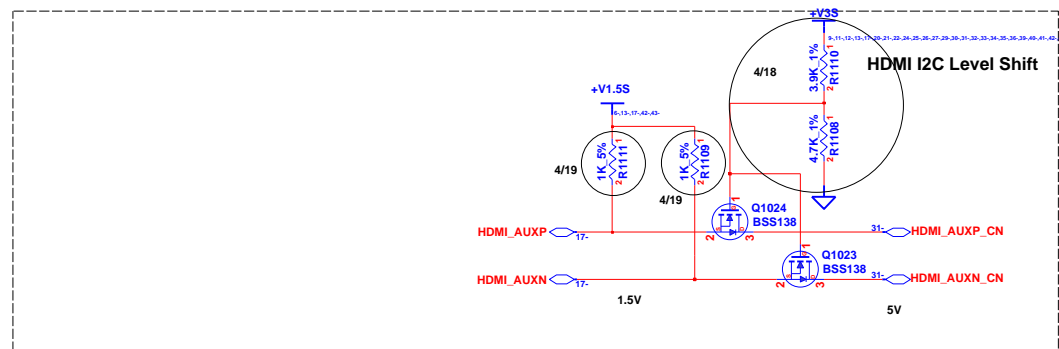
CHANGE by *KarenShen* 2-Mar-2011



# HDMI



	HDMI_HPD_CN
Plug Cable	H
Unplug Cable	L



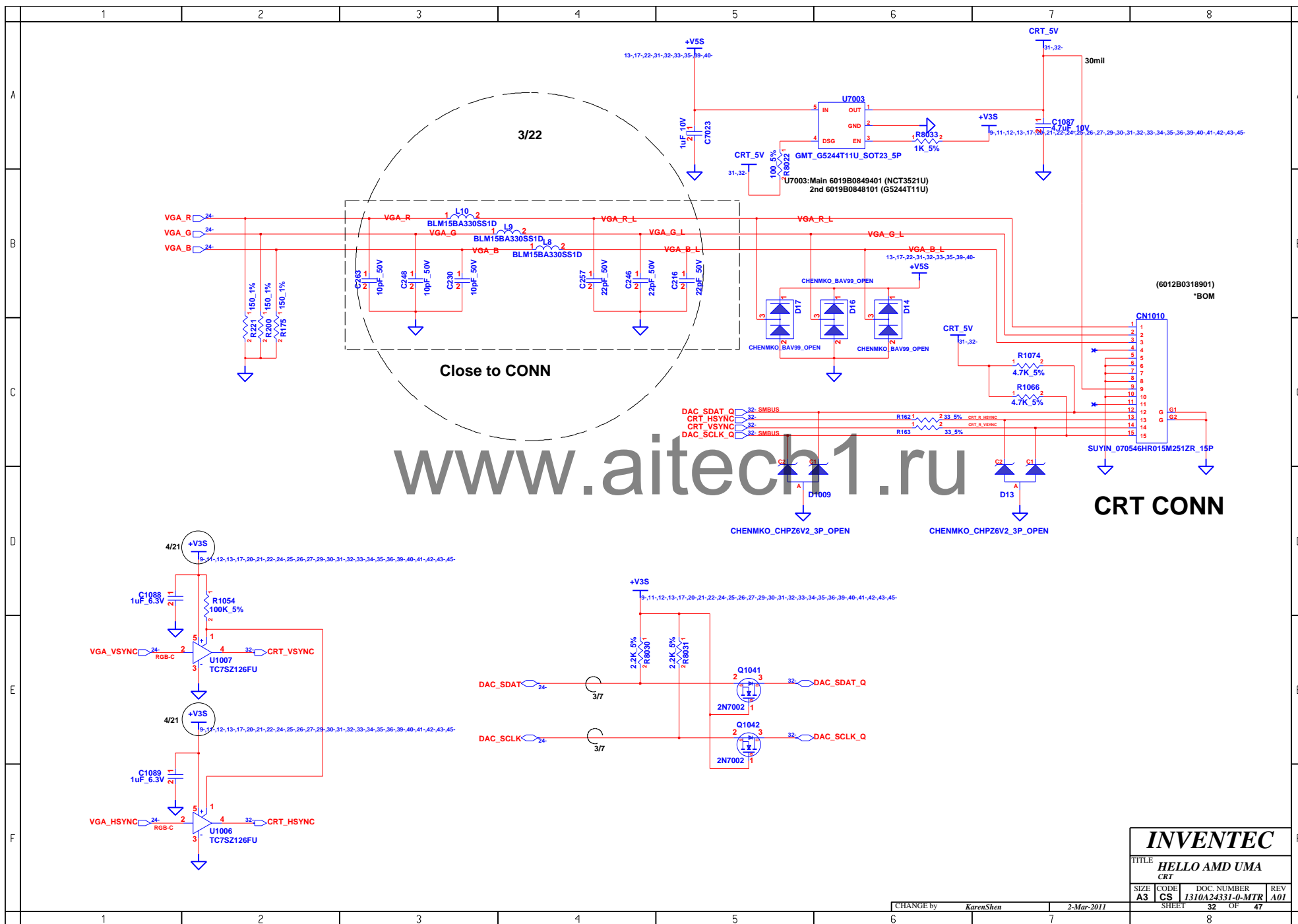
**INVENTEC**

TITLE: **HELLO AMD UMA**  
HDMI

SIZE: **A3** CODE: **CS** DOC. NUMBER: **1310A24331-0-MTR** REV: **A01**

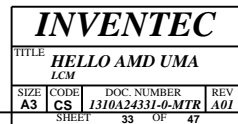
CHANGE by: **KarenShen** 2-Mar-2011

SHEET: **31** OF: **47**

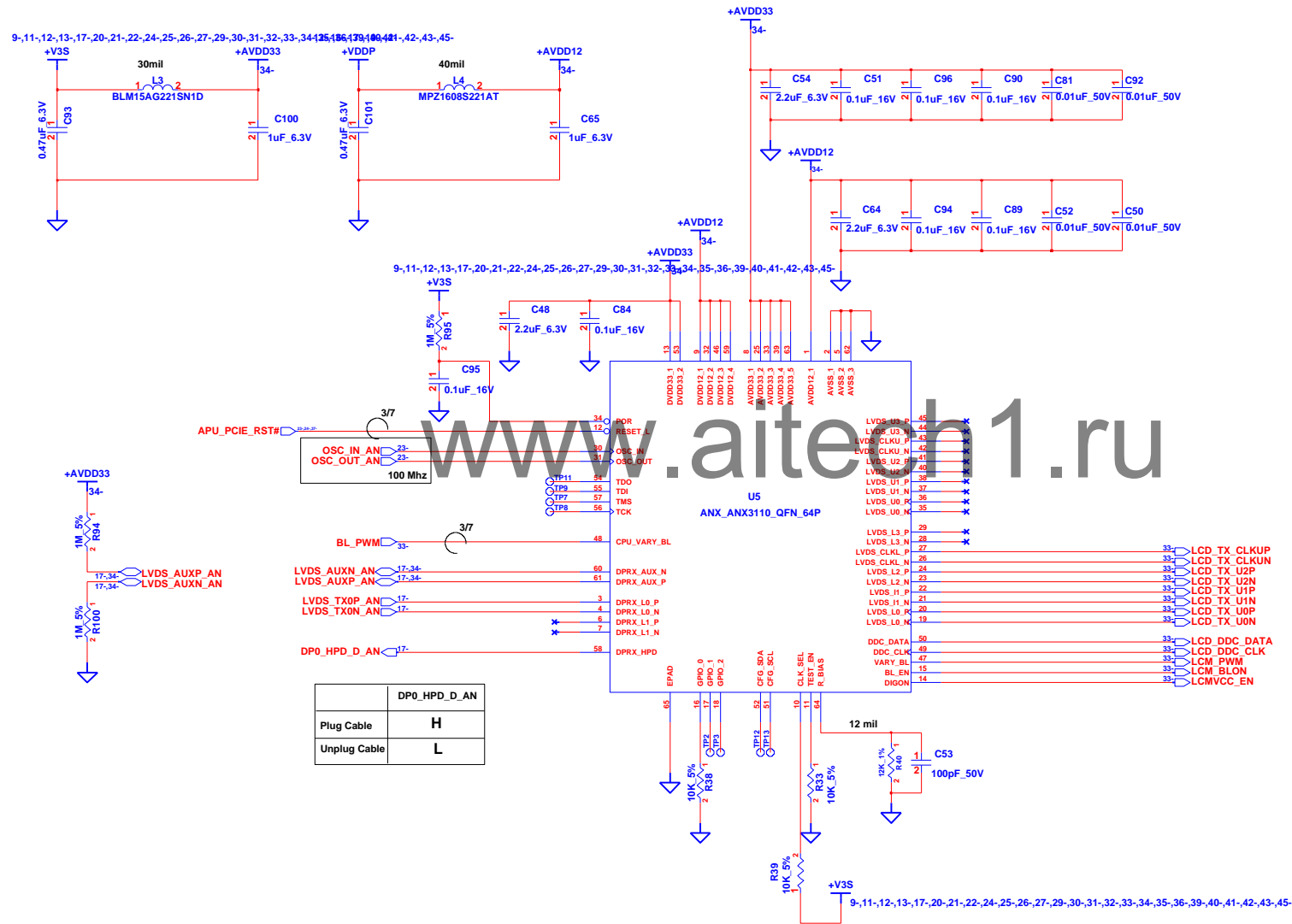




### LCM CONN (40pin)



# eDP TO LVDS IC - ANX3110



	DP0_HPD_D_AN
Plug Cable	H
Unplug Cable	L

**INVENTEC**

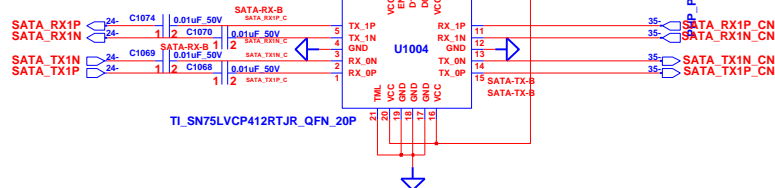
TITLE: **HELLO AMD UMA**  
ANX3110

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24331-0-MTR	A01

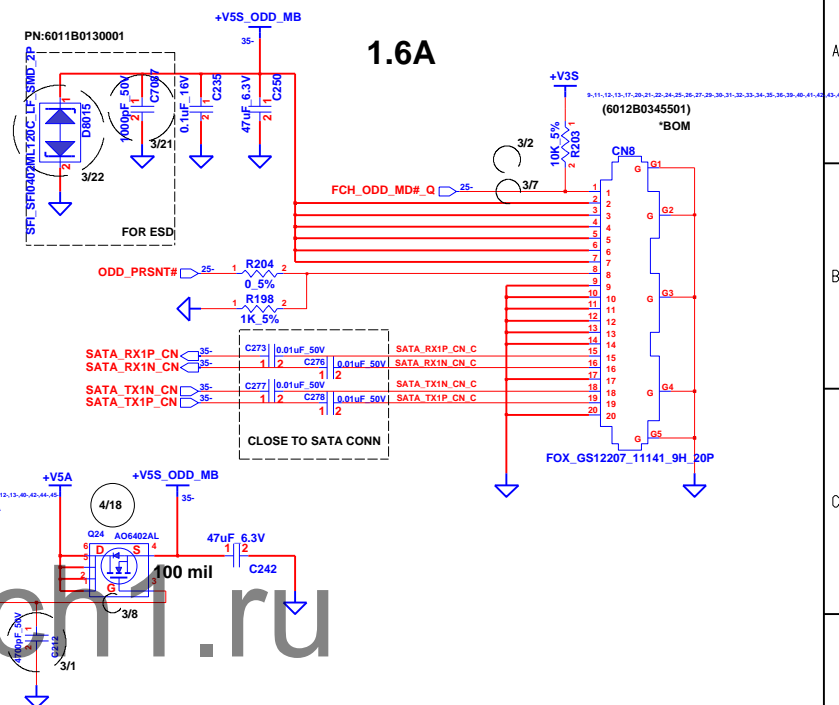
CHANGE by: Karen Shen 2-Mar-2011

SHEET 34 OF 47

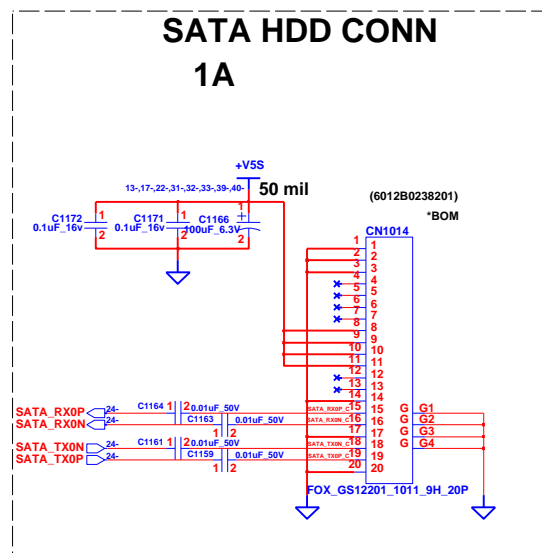
Schematic diagram of the SATA RX/TX signal path. The diagram shows two input multiplexers, C1074 and C1069, selecting between SATA\_RX1P, SATA\_RX1N and SATA\_TX1N, SATA\_TX1P signals. These are connected to a U1004 buffer. The buffer outputs are connected to the RX and TX pins of the TI\_SN75LVCP412RJT\_QFN\_20P transceiver. The transceiver also has pins for TMUX, VCC, GND, and VCC. The output of the transceiver is connected to the SATA\_RX1P\_CN, SATA\_RX1N\_CN, SATA\_TX1N\_CN, and SATA\_TX1P\_CN pins.



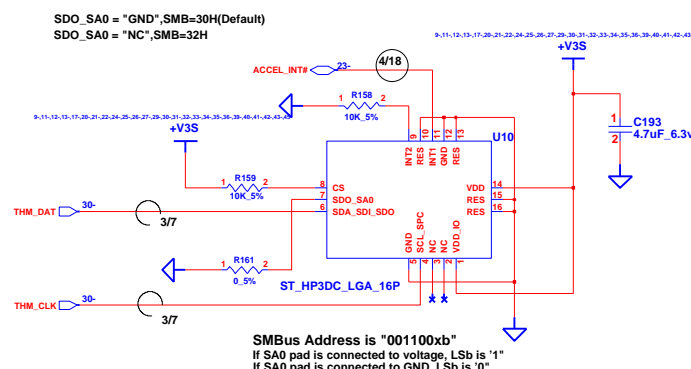
### 1.6A



**1A**



**HARDDRIVE PROTECTION**  
**P/N = 6019B0800501**



**SMBus Address is "001100xb"**  
If SA0 pad is connected to voltage, LSb is '1'  
If SA0 pad is connected to GND, LSb is '0'

**INVENTEC**

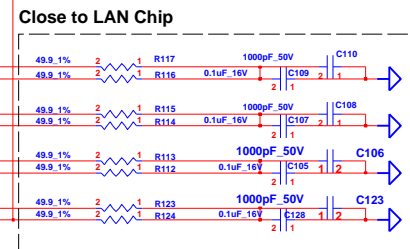
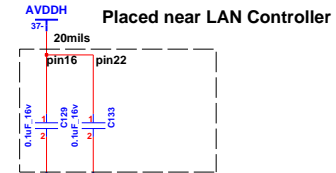
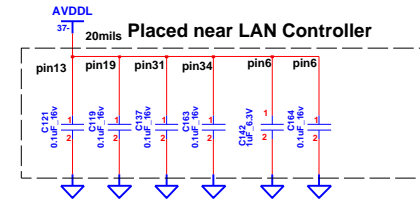
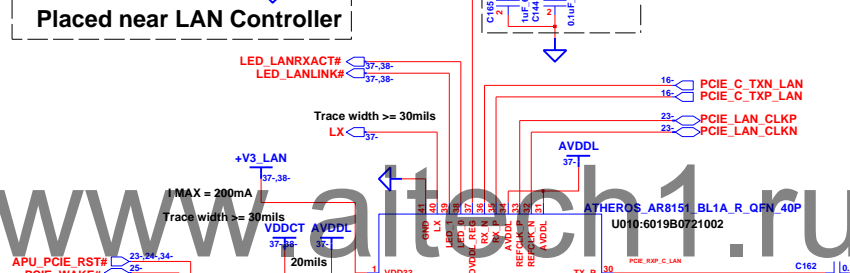
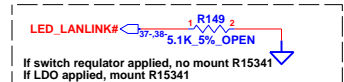
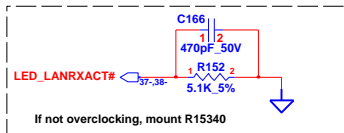
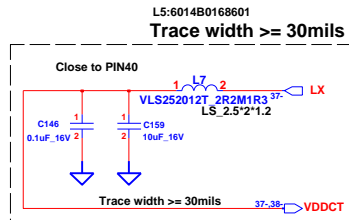
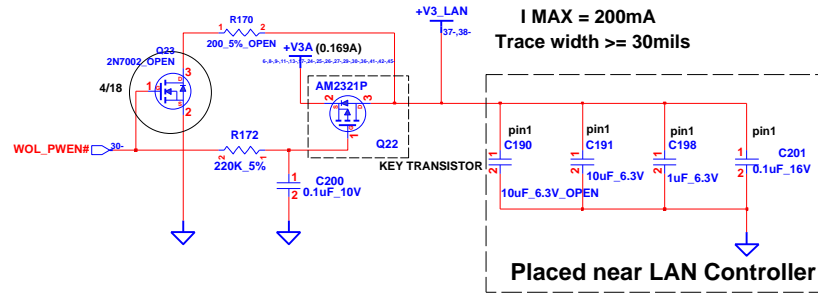
TITLE			
<b>HELLO AMD UMA</b> SATA HDD & ODD CONN			
SIZE	CODE	DOC. NUMBER	REV
<b>A3</b>	<b>CS</b>	<b>1310A24331-0-MTR</b>	<b>A01</b>

## A

## A

FF

# Giga LAN - AR8151



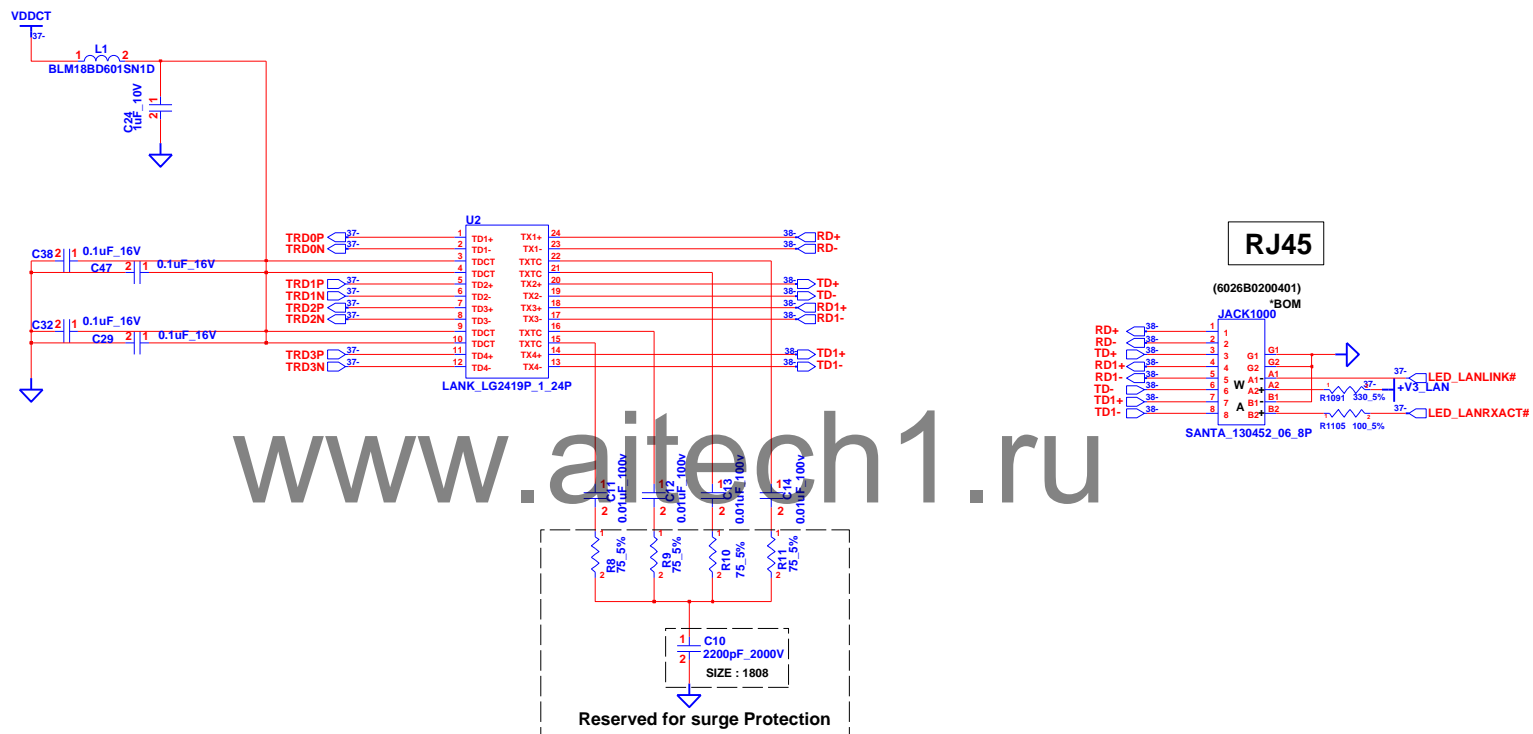
**INVENTEC**

TITLE: **HELLO AMD UMA**  
LAN-AR8151

SIZE: **A3** CODE: **CS** DOC. NUMBER: **1310A24331-0-MTR** REV: **A01**

CHANGE by: **KarenShen** 2-Mar-2011

SHEET: **37** OF: **47**



LAYOUT NOTE : Place termination resistors and caps as close to LAN controller as possible

**INVENTEC**

TITLE  
**HELLO AMD UMA**  
RJ45 CONN

SIZE CODE DOC. NUMBER REV  
**A3 CS 1310A24331-0-MTR A01**

CHANGE by KarenShen 2-Mar-2011

SHEET 38 OF 47

# AUDIO CODEC - 92HD80B

**Close to Pin3**

**Close to Pin9**

**Close to Pin1**

**Close to Audio Codec**

**INT-SPEAKER CONN**

PORT	Discription	Sense
A	NO USE	
B	Headphone	HPS
C	Microphone	MICS
D	SPKR	
E	NO USE	
F	NO USE	

**INVENTEC**

**HELLO AMD UMA**

**AUDIO CODEC & SPEAKER CONN**

SIZE: A3 CS CODE: 1310A24331-0-MTR REV: A01

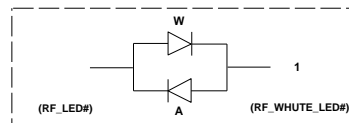
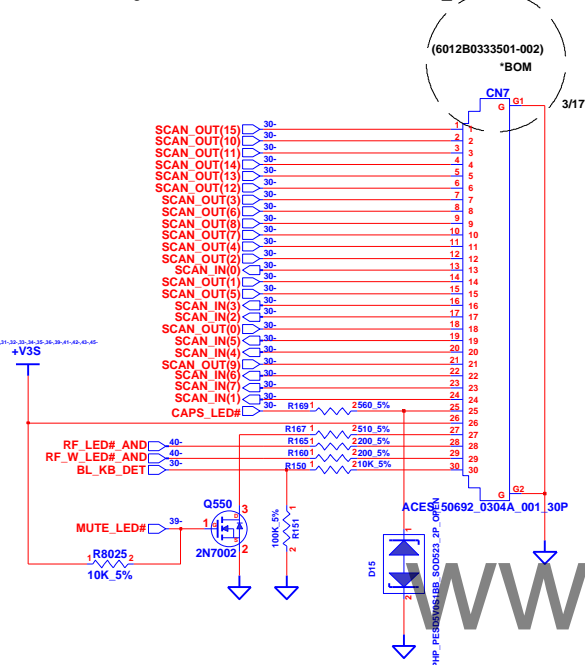
SHEET: 39 OF 47

PORT	Discription	Sense
A	NO USE	
B	Headphone	HPS
C	Microphone	MICS
D	SPKR	
E	NO USE	
F	NO USE	

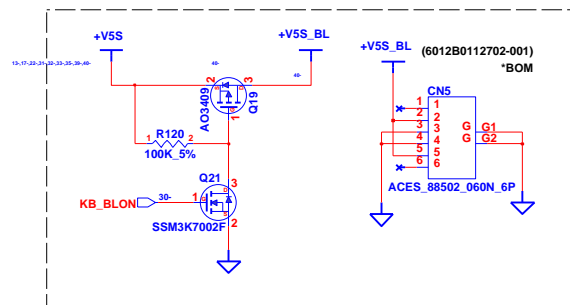
## INT-SPEAKER CONN

<b>INVENTEC</b>			
TITLE <b>HELLO AMD UMA</b> AUDIO CODEC & SPEAKER CONN			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A24331-0-MTR</b>	REV <b>A01</b>
SHEET <b>39</b>		OF <b>47</b>	

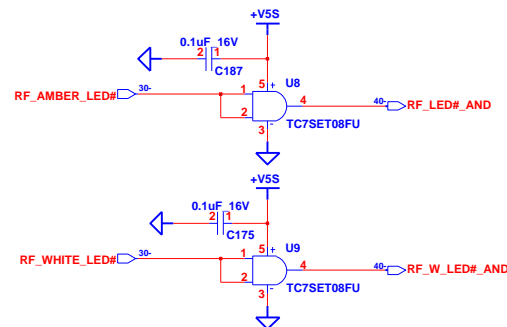
# KeyBoard CONN (30 pin)



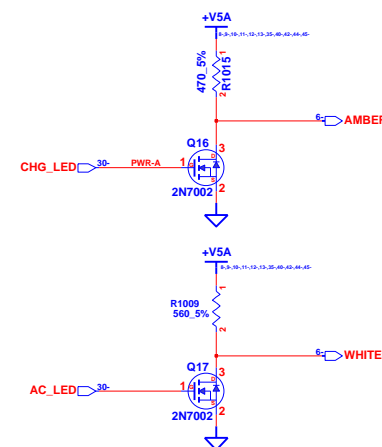
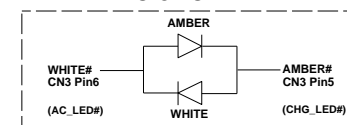
## KB BL



## RF LED



## DC-JACK LED



## INVENTEC

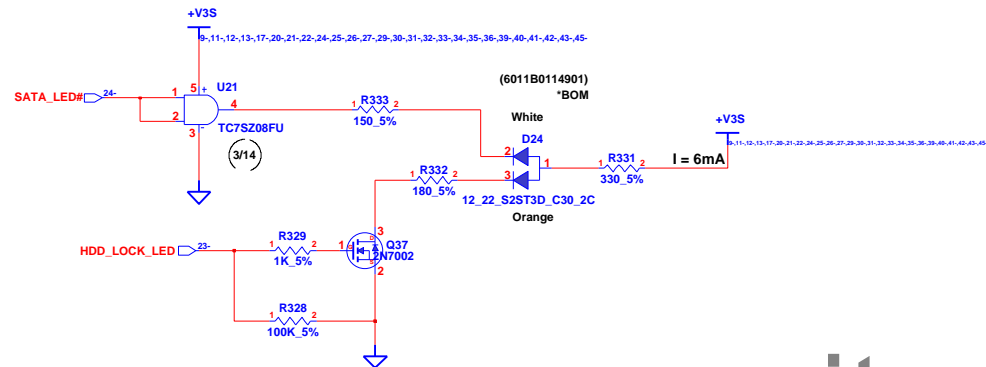
TITLE: HELLO AMD UMA			
KEYBOARD CONN & INDICATE LED			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A24331-0-MTR	REV: A01
SHEET: 40		OF: 47	

CHANGE by: KarenShen 2-Mar-2011

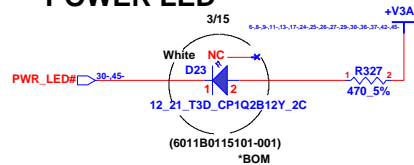


# SATA LED & POWER LED

## SATA LED & HDD-HALTED LED



## POWER LED



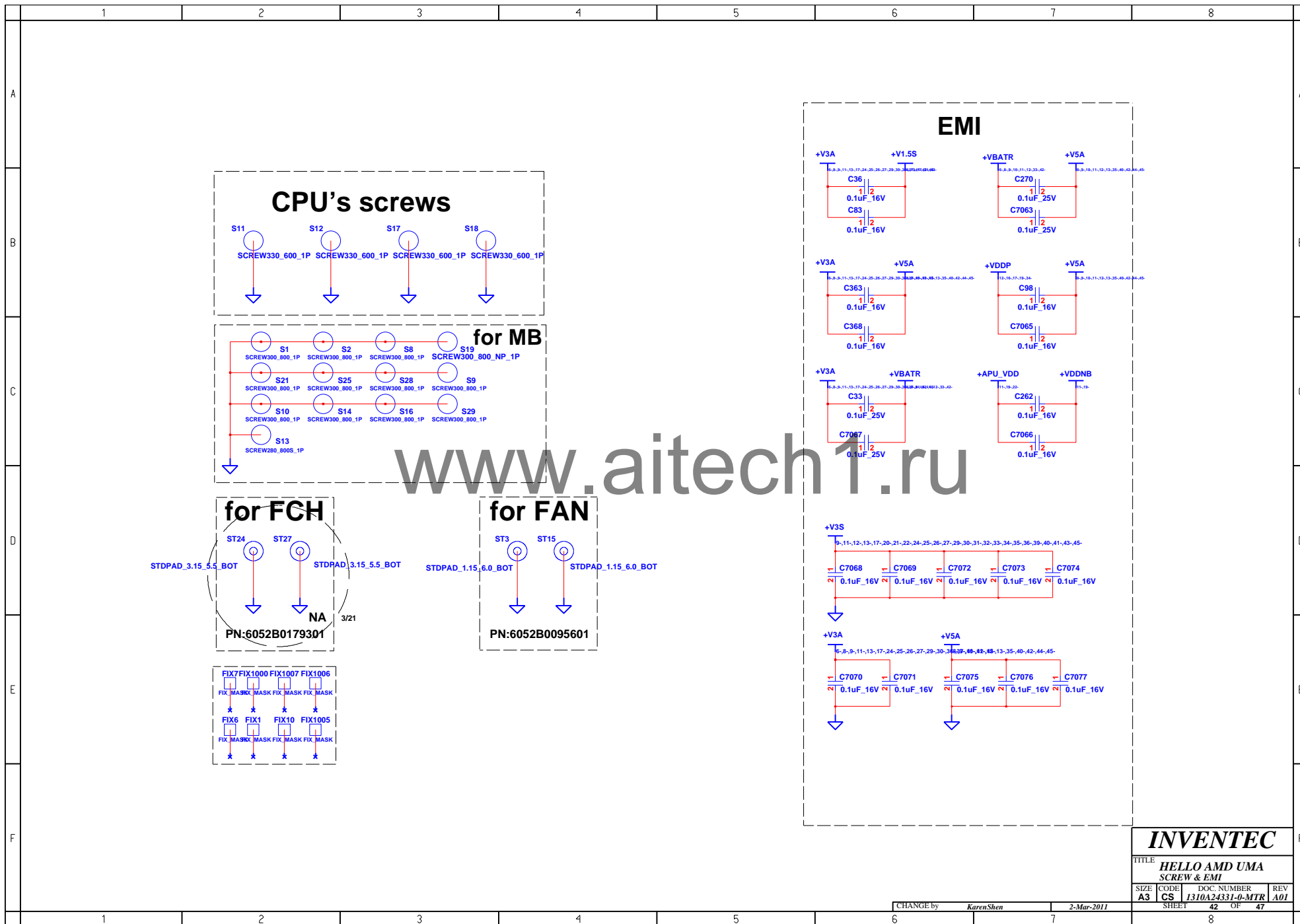
www.aitech1.ru

**INVENTEC**

TITLE			
HELLO AMD UMA			
SATA LED & PWR LED			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24331-0-MTR	A01
SHEET		41	OF 47

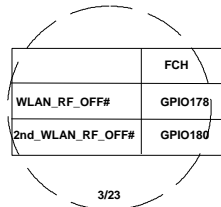
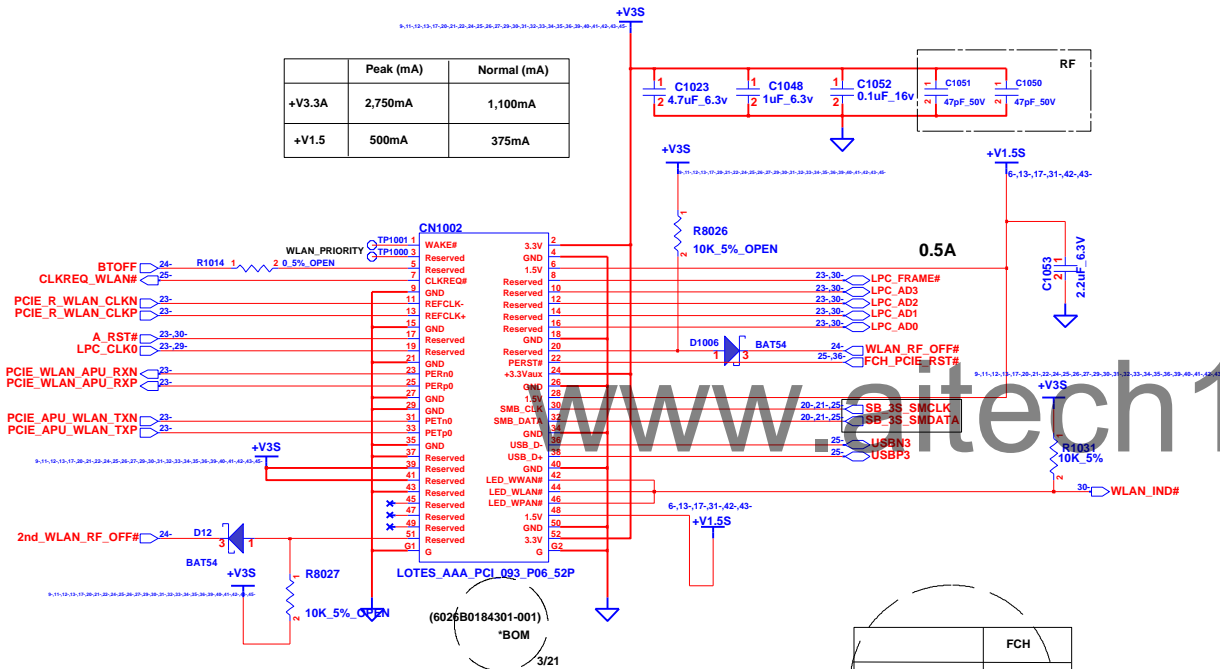
CHANGE by Karen Shen 2-Mar-2011

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# WLAN CONN (MINICARD)

	Peak (mA)	Normal (mA)
+V3.3A	2,750mA	1,100mA
+V1.5	500mA	375mA



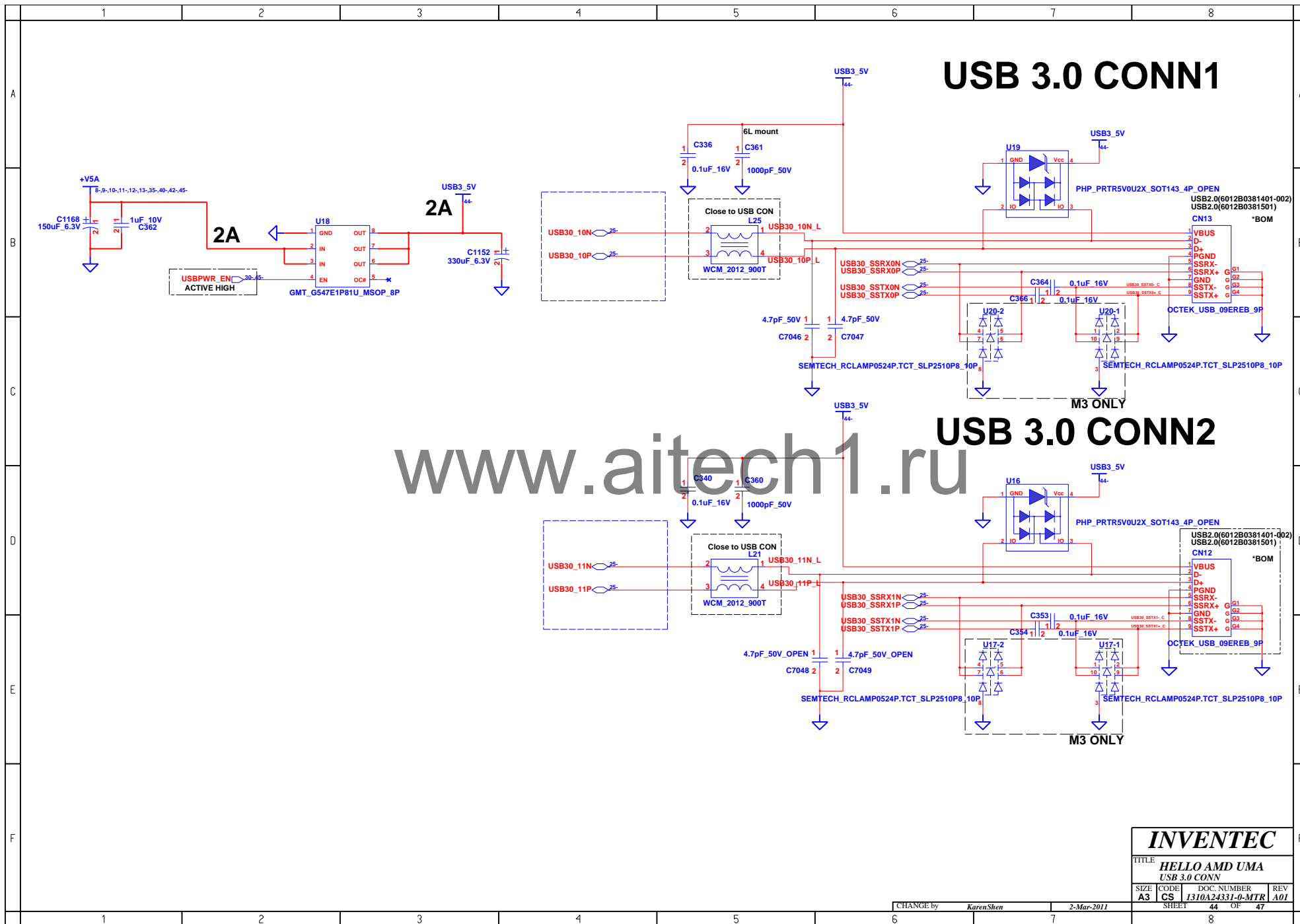
**INVENTEC**

TITLE  
**HELLO AMD UMA  
WLAN & BT**

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A24331-0-MTR</b>	REV <b>A01</b>
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CHANGE by **KarenShen** 2-Mar-2011

SHEET **43** OF **47**



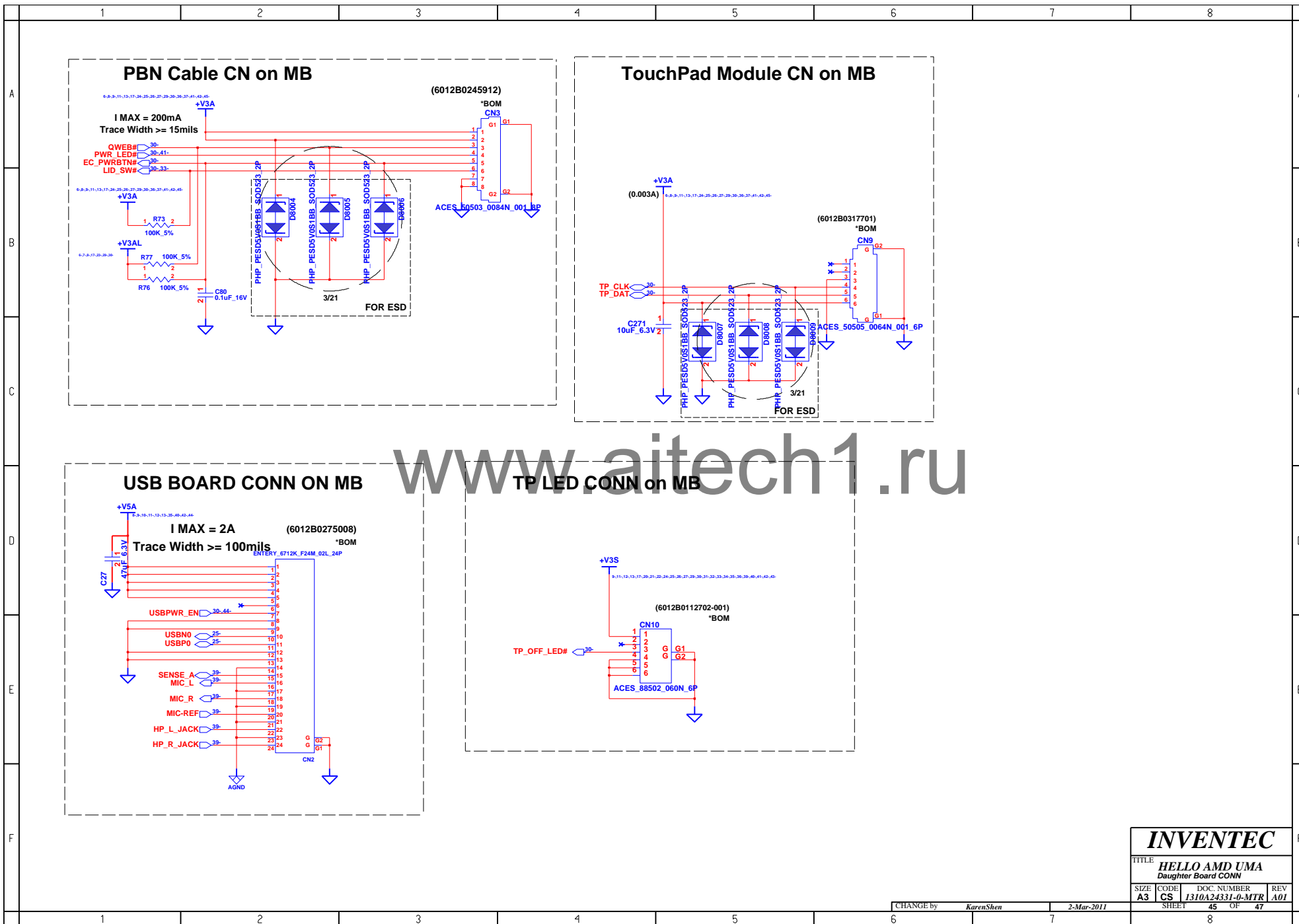
**INVENTEC**

TITLE: **HELLO AMD UMA**  
USB 3.0 CONN

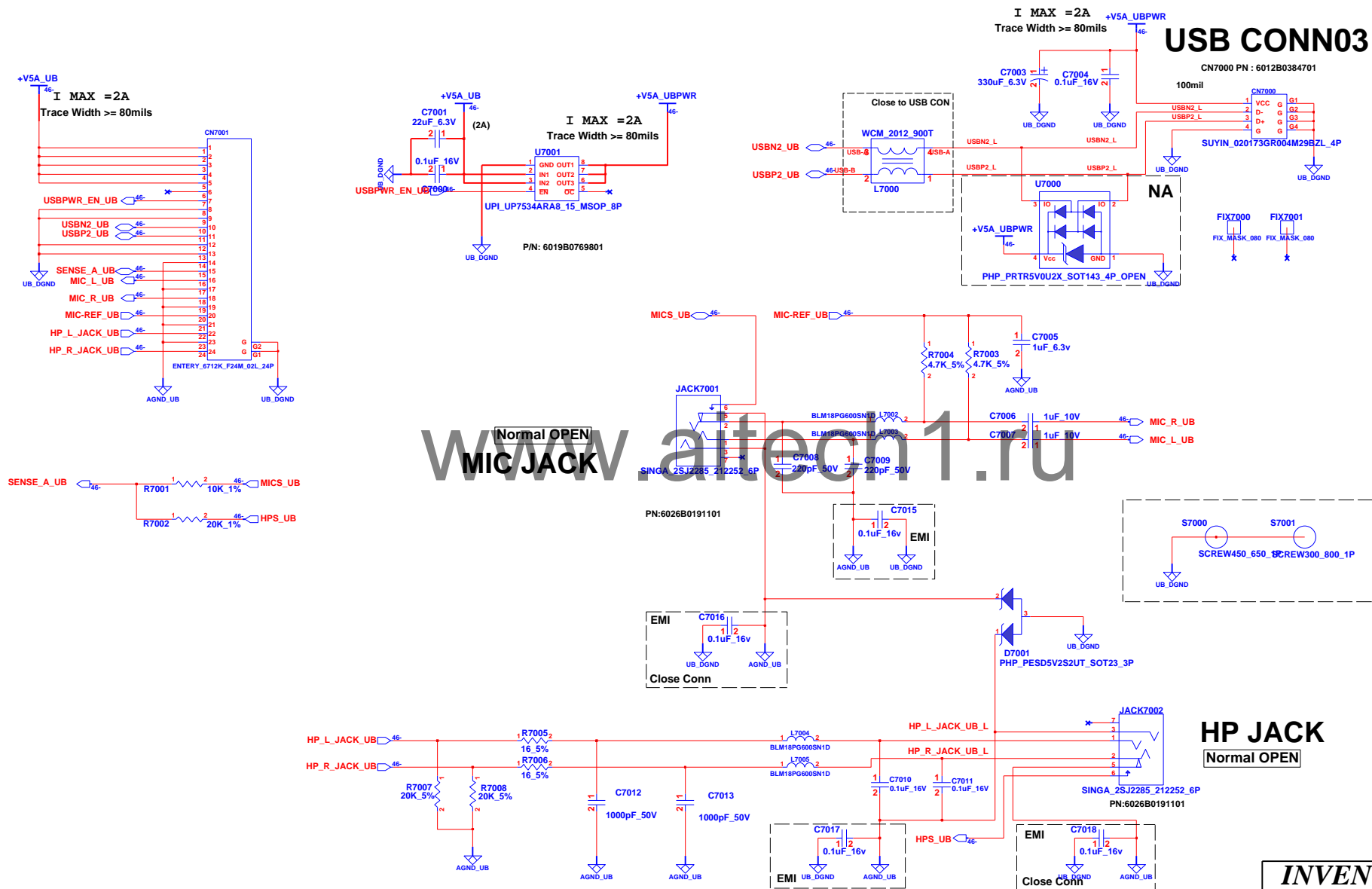
SIZE: **A3** CODE: **CS** DOC. NUMBER: **1310A24331-0-MTR** REV: **A01**

CHANGE by: **KarenShen** 2-Mar-2011

SHEET: **44** OF: **47**



# USB + AUDIO BOARD

**INVENTEC**

TITLE	<b><i>HELLO AMD UMA</i></b>
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SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A24331-0-MTR</b>	REV <b>A01</b>
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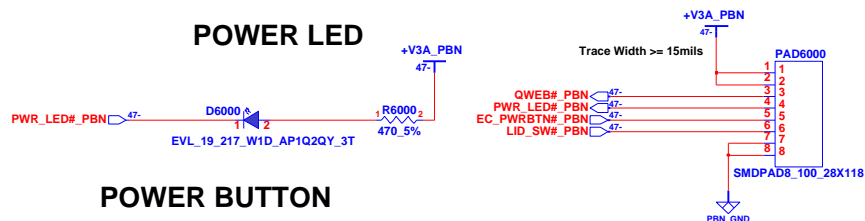
AS	SS	1510/12-4551-6-MIR	AG1
SHEET		46	OF 47

CHANGE by	<i>Karen Shen</i>	<i>2-Mar-2011</i>
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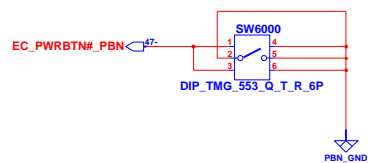
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# POWER BOTTON BOARD

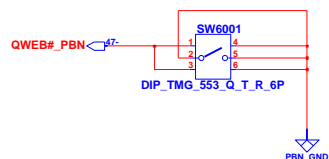
## POWER LED



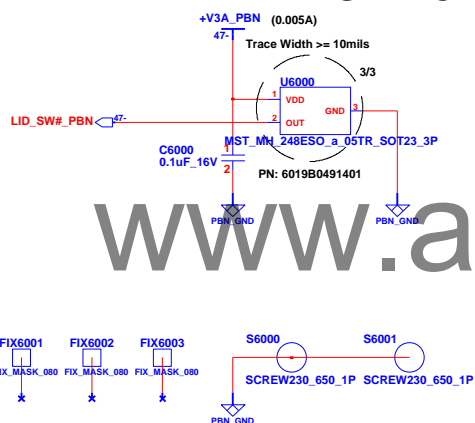
## POWER BUTTON



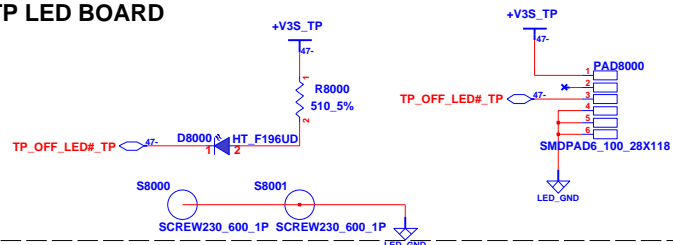
## QWEB BUTTON



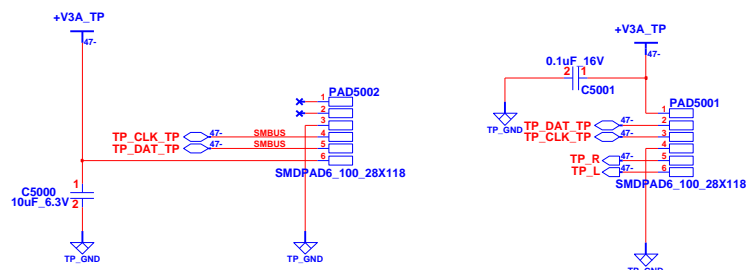
## LID SWITCH



## TP LED BOARD

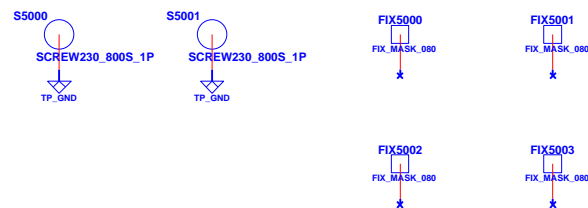


# PICK BUTTON BOARD



## Left side

## Right side



**INVENTEC**

TITLE  
HELLO AMD UMA

SIZE CODE DOC NUMBER REV  
A3 CS 1310A24331-0-MTR A01

CHANGE by KarenShen 2-Mar-2011

SHEET 47 OF 47